Octal PMBus Power Supply Monitor and Controller with EEPROM

FEATURES

- PMBus Compliant Interface and Command Set
- Configuration EEPROM
- Fault Logging to Internal EEPROM
- Differential Input, 15-Bit ΔΣ ADC with Less Than ±0.25% of Total Unadjusted Error
- Monitors Eight Output Channels and One Input Voltage
- 8-Channel Sequencer
- Programmable Watchdog Timer
- Eight UV/OV Voltage Supervisors
- Eight 10-Bit Voltage-Buffered IDACs with Soft Connect
- Linear, Voltage Servo Adjusts Supply Voltages by Ramping Voltage-Buffered IDAC Outputs Up/Down
- Supports Multichannel Fault Management
- On-Chip Digital Temperature Sensor
- Available in 64-Pin 9mm × 9mm QFN Package

APPLICATIONS

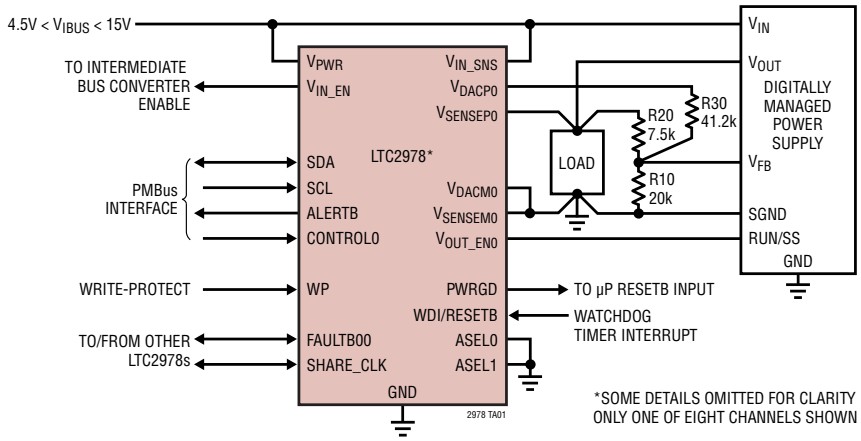
- Computers
- Network Servers

DESCRIPTION

The LTC®2978 is an octal, PMBus compliant power supply monitor, supervisor, sequencer and margin controller. PMBus functions include warning and fault OV/UV threshold pairs for eight output channels and one input channel. Programmable fault response allows the power supplies to be disabled with optional retry after a fault has been detected. PMBus reads allow eight output voltages and one input voltage to be monitored. In addition, odd numbered channels can substitute sense resistor voltage measurements for output voltage measurements. PMBus commands support power supply sequencing and precision point-of-load voltage servo to one of three programmed values: margin high, margin low and nominal. A programmable watchdog timer monitors microprocessor activity for a stalled condition and resets the micro if necessary. The 1-wire synchronization bus supports power supply sequencing across multiple LTC2978 devices. User programmable parameters can be stored in EEPROM. Voltage supervisor, voltage monitor and temperature faults can also be logged to EEPROM.

TYPICAL APPLICATION

Octal Power Supply Controller with PMBus Interface



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ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltages:
- V_{PWR} to GND ..... –0.3V to 15V
- V_{IN_SNS} to GND ..... –0.3V to 15V
- V_{DD33} to GND ..... –0.3V to 3.6V
- V_{DD25} to GND ..... –0.3V to 2.75V

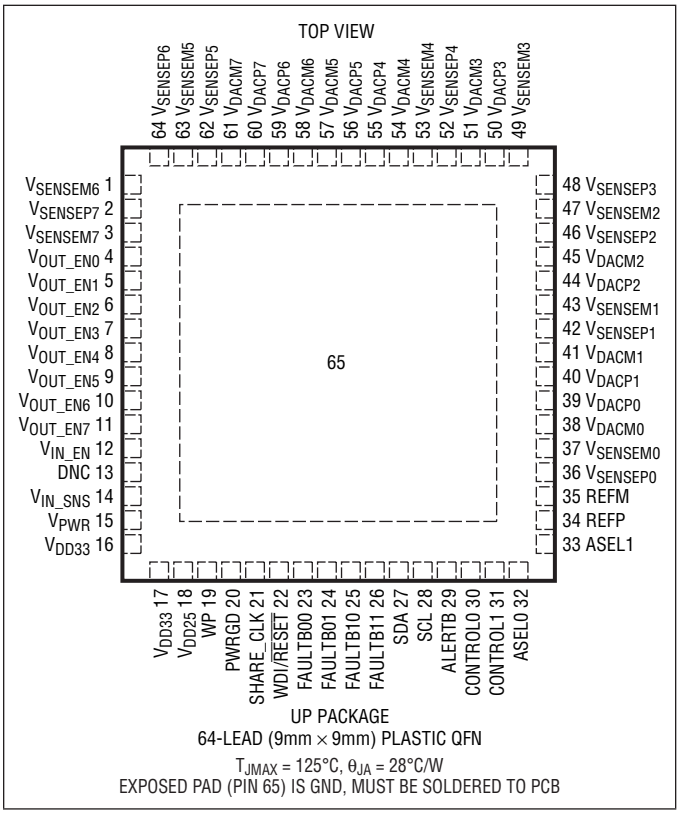
Digital Input/Output Voltages:
- ALERTB, SDA, SCL, CONTROL0, CONTROL1..... –0.3V to 5.5V
- PWRGD, SHARE_CLK, WDI, WP .....–0.3V to V_{DD33} + 0.3V
- FAULTB00, FAULTB01, FAULTB10, FAULTB11 .....–0.3V to V_{DD33} + 0.3V
- ASEL0, ASEL1.....–0.3V to V_{DD33} + 0.3V

Analog Voltages:
- REFP..... –0.3V to 1.35V
- REFM to GND..... –0.3V to 0.3V
- $V_{SENSEP[7:0]}$ to GND..... –0.3V to 6V
- $V_{SENSEM[7:0]}$ to GND ..... –0.3V to 6V
- $V_{OUT\_EN[3:0]}$, V_{IN_EN} to GND ..... –0.3V to 15V
- $V_{OUT\_EN[7:4]}$ to GND..... –0.3V to 6V
- $V_{DACP[7:0]}$ to GND ..... –0.3V to 6V
- $V_{DACM[7:0]}$ to GND ..... –0.3V to 0.3V

Operating Temperature Range:
- LTC2978C..... 0°C to 70°C
- LTC2978I .....–40°C to 85°C

Storage Temperature Range ..... –65°C to 125°C

PIN CONFIGURATION



UP PACKAGE
64-LEAD (9mm × 9mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 28°C/W
EXPOSED PAD (PIN 65) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2978CUP#PBF	LTC2978CUP#TRPBF	LTC2978	64-Lead (9mm × 9mm) Plastic QFN	0°C to 70°C
LTC2978IUP#PBF	LTC2978IUP#TRPBF	LTC2978	64-Lead (9mm × 9mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{PWR} = V_{IN_SNS} = 12V, V_{DD33}, V_{DD25} and REF pins floating, unless otherwise indicated. C_{VDD33} = 100nF, C_{VDD25} = 100nF and C_{REF} = 100nF.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power-Supply Characteristics							
V_{PWR}	V_{PWR} Supply Input Operating Range		●	4.5		15	V
I_{PWR}	V_{PWR} Supply Current	4.5V ≤ V_{PWR} ≤ 15V, V_{DD33} Floating	●		10	13	mA
I_{VDD33}	V_{DD33} Supply Current	3.13V ≤ V_{DD33} ≤ 3.47V, V_{PWR} = V_{DD33}	●		10	13	mA
V_{UVLO_VDD33}	V_{DD33} Undervoltage Lockout	V_{DD33} Ramping Up, V_{PWR} = V_{DD33}	●	2.35	2.55	2.8	V
	V_{DD33} Undervoltage Lockout Hysteresis				120		mV
V_{DD33}	Supply Input Operating Range	V_{PWR} = V_{DD33}	●	3.13		3.47	V
	Regulator Output Voltage	4.5V ≤ V_{PWR} ≤ 15V	●	3.13	3.26	3.47	V
	Regulator Output Short-Circuit Current	V_{PWR} = 4.5V, V_{DD33} = 0V	●	75	90	140	mA
V_{DD25}	Regulator Output Voltage	3.13V ≤ V_{DD33} ≤ 3.47V	●	2.35	2.5	2.6	V
	Regulator Output Short-Circuit Current	V_{PWR} = V_{DD33} = 3.47V, V_{DD25} = 0V	●	30	55	80	mA
Voltage Reference Characteristics							
V_{REF}	Output Voltage				1.232		V
	Temperature Coefficient				3		ppm/°C
	Hysteresis	(Note 3)			100		ppm
ADC Characteristics							
V_{IN_ADC}	Voltage Sense Input Range	Differential Voltage: V_{IN_ADC} = ($V_{SENSEPn}$ – $V_{SENSEMn}$)	●	0		6	V
		Single-Ended Voltage: $V_{SENSEMn}$	●	–0.1		0.1	V
	Current Sense Input Range (Odd Numbered Channels Only When So Configured)	Single-Ended Voltage: $V_{SENSEPn}$, $V_{SENSEMn}$	●	–0.1		6	V
		Differential Voltage: V_{IN_ADC}	●	–170		170	mV
N_ADC	Voltage Sense Resolution	0V ≤ V_{IN_ADC} ≤ 6V			122		µV/LSB
	Current Sense Resolution (Odd Numbered Channels Only When So Configured)	0mV ≤ |V_{IN_ADC}| < 16mV 16mV ≤ |V_{IN_ADC}| < 32mV 32mV ≤ |V_{IN_ADC}| < 63.9mV 63.9mV ≤ |V_{IN_ADC}| < 127.9mV 127.9mV ≤ |V_{IN_ADC}|			15.625 31.25 62.5 125 250		µV/LSB µV/LSB µV/LSB µV/LSB µV/LSB
TUE_ADC	Total Unadjusted Error	V_{IN_ADC} ≥ 1.8V (Note 4)	●			±0.25	%
INL_ADC	Integral Nonlinearity	Voltage Sense Mode (Note 5)	●			±854	µV
		Current Sense Mode, Odd Numbered Channels Only, 15.6µV/LSB (Note 5)	●			±31.3	µV
DNL_ADC	Differential Nonlinearity	Voltage Sense Mode	●			±400	µV
		Current Sense Mode, Odd Numbered Channels Only	●			±31.3	µV
V_{OS_ADC}	Offset Error	Voltage Sense Mode	●			±250	µV
		Current Sense Mode, Odd Numbered Channels Only	●			±35	µV
GAIN_ADC	Gain Error	Voltage Sense Mode, V_{IN_ADC} = 6V	●			±0.2	%
		Current Sense Mode, Odd Numbered Channels Only, V_{IN_ADC} = ±0.17V	●			±0.2	%
t_{CONV_ADC}	Conversion Time	Voltage Sense Mode (Note 6)			6.15		ms
		Current Sense Mode (Note 6)			24.6		ms
		Temperature Input (Note 6)			24.6		ms
C_{IN_ADC}	Input Sampling Capacitance				1		pF
f_{IN_ADC}	Input Sampling Frequency				62.5		kHz

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
I_{IN_ADC}	Input Leakage Current	V_{IN_ADC} = 0V, 0V ≤ $V_{COMMONMODE}$ ≤ 6V, Current Sense Mode		●			±0.5	µA
	Differential Input Current	V_{IN_ADC} = 0.17V, Current Sense Mode		●		80	250	nA
		V_{IN_ADC} = 6V, Voltage Sense Mode		●		10	15	µA
Voltage Buffered IDAC Output Characteristics								
N_V_{DACP}	Resolution					10		Bits
V_{FS_VDACP}	Full-Scale Output Voltage (Programmable)	DAC Code = 0x3FF, DAC Polarity = 1	Buffer Gain Setting_0	● ●	1.32 2.53	1.38 2.65	1.44 2.77	V V
INL_V_{DACP}	Integral Nonlinearity	(Note 7)		●			±2	LSB
DNL_V_{DACP}	Differential Nonlinearity	(Note 7)		●			±2.4	LSB
V_{OS_VDACP}	Offset Voltage	(Note 7)		●			±10	mV
V_{DACP}	Load Regulation (V_{DACPn} – V_{DACMn})	V_{DACPn} = 2.65V, I_{VDACPn} Sourcing = 2mA				100		ppm/mA
		V_{DACPn} = 0.1V, I_{VDACPn} Sinking = 2mA				100		ppm/mA
	PSRR (V_{DACPn} – V_{DACMn})	DC: 3.13V ≤ V_{DD33} ≤ 3.47V, V_{PWR} = V_{DD33}				60		dB
		100mV Step in 20ns with 50pF Load				40		dB
	DC CMRR (V_{DACPn} – V_{DACMn})	–0.1V ≤ V_{DACMn} ≤ 0.1V				60		dB
	Leakage Current	V_{DACPn} Hi-Z, 0V ≤ V_{DACPn} ≤ 6V		●			±100	nA
	Short-Circuit Current Low	V_{DACPn} Shorted to GND		●	–10		–4	mA
	Short-Circuit Current High	V_{DACPn} Shorted to V_{DD33}		●	4		10	mA
C_{OUT}	Output Capacitance	V_{DACPn} Hi-Z				10		pF
t_{S_VDACP}	DAC Output Update Rate	Fast Servo Mode				250		µs
Voltage Supervisor Characteristics								
V_{IN_VS}	Input Voltage Range (Programmable)	V_{IN_VS} = ($V_{SENSEPn}$ – $V_{SENSEMn}$)	Low Resolution Mode High Resolution Mode	● ●	0 0		6 3.8	V V
		Single-Ended Voltage: $V_{SENSEMn}$		●	–0.1		0.1	V
N_VS	Voltage Sensing Resolution	0V to 3.8V Range: High Resolution Mode				4		mV/LSB
		0V to 6V Range: Low Resolution Mode				8		mV/LSB
TUE_VS	Total Unadjusted Error	2V ≤ V_{IN_VS} ≤ 6V, Low Resolution Mode		●			±1.25	%
		1.5V < V_{IN_VS} ≤ 3.8V, High Resolution Mode		●			±1.0	%
		0.8V ≤ V_{IN_VS} ≤ 1.5V, High Resolution Mode		●			±1.5	%
t_{S_VS}	Update Rate					12.21		µs
V_{IN_SNS} Input Characteristics								
V_{VIN_SNS}	V_{IN_SNS} Input Voltage Range			●	0		15	V
R_{VIN_SNS}	V_{IN_SNS} Input Resistance			●	70	90	110	kΩ
TUE_{VIN_SNS}	V_{IN_ON}, V_{IN_OFF} Threshold Total Unadjusted Error	3V ≤ V_{VIN_SNS} ≤ 8V		●			±2.0	%
		V_{VIN_SNS} > 8V		●			±1.0	%
	READ_V_{IN} Total Unadjusted Error	3V ≤ V_{VIN_SNS} ≤ 8V		●			±1.5	%
		V_{VIN_SNS} > 8V		●			±1.0	%
Voltage Buffered IDAC Soft-Connect Comparator Characteristics								
V_{OS_CMP}	Offset Voltage			●		±3	±18	mV
Temperature Sensor Characteristics								
TUE_TS	Total Unadjusted Error					±1		°C
V_{OUT} Enable Output (V_{OUT_EN} [3:0]) Characteristics								
V_{VOUT_ENn}	Output High Voltage	I_{VOUT_ENn} = –5µA, V_{DD33} = 3.3V		●	11.6	12.5	14.7	V

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{VOUT_ENn}	Output Sourcing Current	V_{VOUT_ENn} Pull-Up Enabled, V_{VOUT_ENn} = 1V	●	–5	–6	–8	µA
	Output Sinking Current	Strong Pull-Down Enabled, V_{VOUT_ENn} = 0.4V	●	3	5	8	mA
		Weak Pull-Down Enabled, V_{VOUT_ENn} = 0.4V	●	33	50	60	µA
	Output Leakage Current	Internal Pull-Up Disabled, 0V ≤ V_{VOUT_ENn} ≤ 15V	●			±1	µA
V_{OUT} Enable Output (V_{OUT_EN} [7:4]) Characteristics							
I_{VOUT_ENn}	Output Sinking Current	Strong Pull-Down Enabled, V_{OUT_ENn} = 0.1V	●	3	6	9	mA
	Output Leakage Current	0V ≤ V_{VOUT_ENn} ≤ 6V	●			±1	µA
V_{IN} Enable Output (V_{IN_EN}) Characteristics							
V_{VIN_EN}	Output High Voltage	I_{VIN_EN} = –5µA, V_{DD33} = 3.3V	●	11.6	12.5	14.7	V
I_{VIN_EN}	Output Sourcing Current	V_{IN_EN} Pull-Up Enabled, V_{VIN_EN} = 1V	●	–5	–6	–8	µA
	Output Sinking Current	Strong Pull-Down Enabled, V_{VIN_EN} = 0.4V	●	3	5	8	mA
		Weak Pull-Down Enabled, V_{VIN_EN} = 0.4V	●	33	50	60	µA
	Leakage Current	Internal Pull-Up Disabled, 0V ≤ V_{VIN_EN} ≤ 15V	●			±1	µA
EEPROM Characteristics							
Endurance	(Note 8)	0°C < T_J < 85°C During EEPROM Write Operations	●	10,000			Cycles
Retention	(Note 8)	T_A < 85°C	●	10			Years
Mass_Write	Mass Write Operation Time (Note 9)	STORE_USER_ALL, 0°C < T_J < 85°C During EEPROM Write Operations	●		440	4100	ms
Digital Inputs SCL, SDA, CONTROL0, CONTROL1, WDI/RESETB, FAULTB00, FAULTB01, FAULTB10, FAULTB11, WP							
V_{IH}	High Level Input Voltage		●	2.1			V
V_{IL}	Low Level Input Voltage		●			1.5	V
V_{HYST}	Input Hysteresis				20		mV
I_{LEAK}	Input Leakage Current	0V ≤ V_{PIN} ≤ 5.5V, SDA, SCL, CONTROLx Pins Only	●			±2	µA
		0V ≤ V_{PIN} ≤ V_{DD33} + 0.3V, FAULTBxx, WDI/RESETB, WP Pins Only	●			±2	µA
t_{SP}	Pulse Width of Spike Suppressed	FAULTBxx, CONTROLx Pins Only			10		µs
		SDA, SCL Pins Only			98		ns
t_{RESETB}	Pulse Width to Assert Reset	$V_{WDI/RESETB}$ ≤ 1.5V	●	300			µs
t_{WDI}	Pulse Width to Reset Watchdog Timer	$V_{WDI/RESETB}$ ≤ 1.5V	●	0.3		200	µs
f_{WDI}	Watchdog Interrupt Input Frequency		●			1	MHz
C_{IN}	Digital Input Capacitance				10		pF
Digital Input SHARE_CLK							
V_{IH}	High Level Input Voltage		●	1.6			V
V_{IL}	Low Level Input Voltage		●			0.8	V
$f_{SHARE\_CLK\_IN}$	Input Frequency Operating Range		●	90		110	kHz
t_{LOW}	Assertion Low Time	V_{SHARE_CLK} < 0.8V	●	0.825		1.1	µs
t_{RISE}	Rise Time	V_{SHARE_CLK} < 0.8V to V_{SHARE_CLK} > 1.6V	●			450	ns
I_{LEAK}	Input Leakage Current	0V ≤ V_{SHARE_CLK} ≤ V_{DD33} + 0.3V	●			±1	µA
C_{IN}	Input Capacitance				10		pF

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Digital Outputs SDA, ALERTB, PWRGD, SHARE_CLK, FAULTB00, FAULTB01, FAULTB10, FAULTB11							
V_{OL}	Digital Output Low Voltage	I_{SINK} = 3mA	●			0.4	V
$f_{SHARE\_CLK\_OUT}$	Output Frequency Operating Range	5.49kΩ Pull-Up to V_{DD33}	●	90	100	110	kHz
Digital Inputs ASEL0,ASEL1							
V_{IH}	Input High Threshold Voltage		●	V_{DD33} – 0.5			V
V_{IL}	Input Low Threshold Voltage		●			0.5	V
$I_{IH,IL}$	High, Low Input Current	ASEL[1:0] = 0, V_{DD33}	●			±95	µA
$I_{IH,Z}$	Hi-Z Input Current		●			±24	µA
C_{IN}	Input Capacitance				10		pF
Serial Bus Timing Characteristics							
f_{SCL}	Serial Clock Frequency (Note 10)		●	10		400	kHz
t_{LOW}	Serial Clock Low Period (Note 10)		●	1.3			µs
t_{HIGH}	Serial Clock High Period (Note 10)		●	0.6			µs
t_{BUF}	Bus Free Time Between Stop and Start (Note 10)		●	1.3			µs
$t_{HD,STA}$	Start Condition Hold Time (Note 10)		●	600			ns
$t_{SU,STA}$	Start Condition Setup Time (Note 10)		●	600			ns
$t_{SU,STO}$	Stop Condition Setup Time (Note 10)		●	600			ns
$t_{HD,DAT}$	Data Hold Time (LTC2978 Receiving Data) (Note 10)		●	0			ns
	Data Hold Time (LTC2978 Transmitting Data) (Note 10)		●	300		900	ns
$t_{SU,DAT}$	Data Setup Time (Note 10)		●	100			ns
t_{SP}	Pulse Width of Spike Suppressed (Note 10)				98		ns
$t_{TIMEOUT\_BUS}$	Time Allowed to Complete any PMBus Command After Which Time SDA Will Be Released and Command Terminated	Longer Timeout = 0 Longer Timeout = 1	● ●		25 200	35 280	ms ms

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating for extended periods may affect device reliability and lifetime.

Note 2: All currents into device pins are positive. All currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified. If power is supplied to the chip via the V_{DD33} pin only, connect V_{PWR} and V_{DD33} pins together.

Note 3: Hysteresis in the output voltage is created by package stress that differs depending on whether the IC was previously at a higher or lower temperature. Output voltage is always measured at 25°C, but the IC is cycled to 85°C or –40°C before successive measurements. Hysteresis is roughly proportional to the square of the temperature change.

Note 4: TUE(%) is defined as:

Gain Error (%) + 100 • (INL + V_{OS})/V_{IN}.

Note 5: Integral nonlinearity (INL) is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve (0V and 6V). The deviation is measured from the center of the quantization band.

Note 6: The time between successive ADC conversions (latency of the ADC) for any given channel is given as: 36.9ms + (6.15ms • number of ADC channels configured in Low Resolution mode) + (24.6ms • number of ADC channels configured in High Resolution mode).

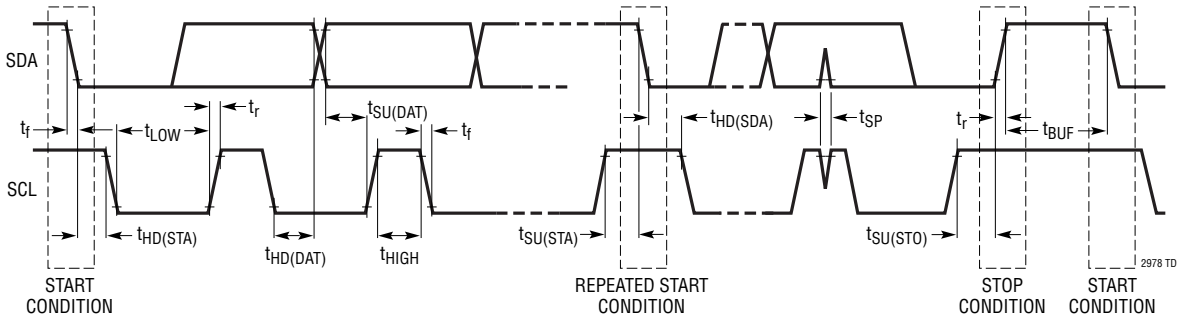
Note 7: Nonlinearity is defined from the first code that is greater than or equal to the maximum offset specification to full-scale code, 1023.

Note 8: EEPROM endurance and retention are guaranteed by design, characterization and correlation with statistical process controls. The minimum retention specification applies for devices whose EEPROM has been cycled less than the minimum endurance specification.

Note 9: The LTC2978 will not acknowledge any PMBus write commands when a STORE_USER_ALL command is being executed.

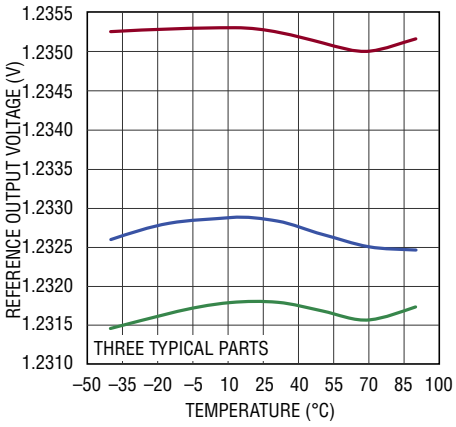
Note 10: Maximum capacitive load, C_B, for SCL and SDA is 400pF. Data and clock rise time (t_r) and fall time (t_f) are: (20 + 0.1• C_B) (ns) < t_r < 300ns and (20 + 0.1 • C_B) (ns) < t_f < 300ns. C_B = capacitance of one bus line in pF. SCL and SDA external pull-up voltage, V_{IO}, is 3.13V < V_{IO} < 5.5V.

TIMING DIAGRAM



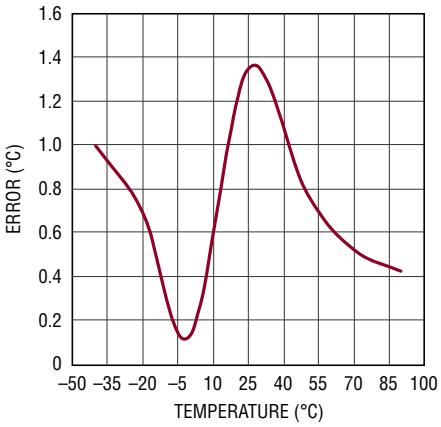
TYPICAL PERFORMANCE CHARACTERISTICS

Reference Voltage vs Temperature



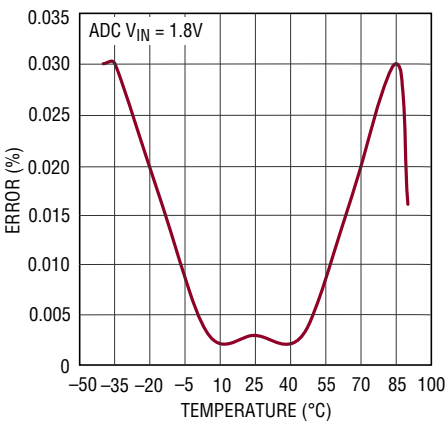
2978 G01

Temperature Sensor Error vs Temperature



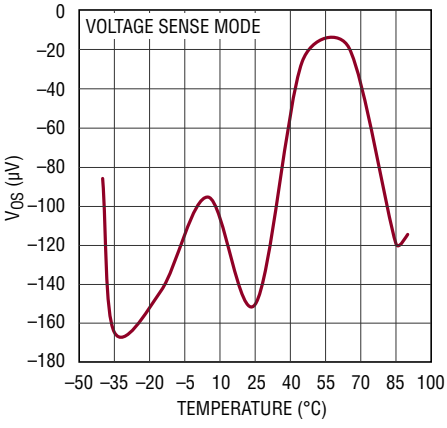
2978 G02

ADC Total Unadjusted Error vs Temperature



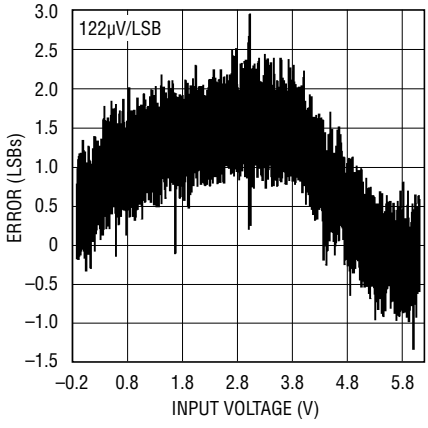
2978 G03

ADC Zero Code Center Offset Voltage vs Temperature



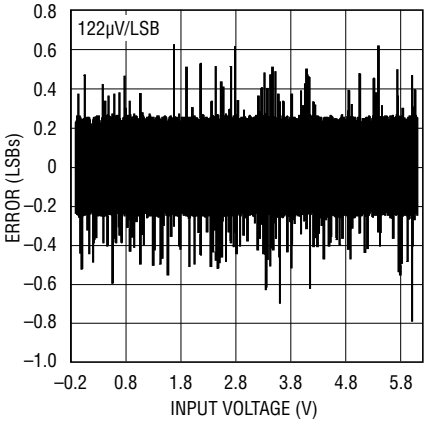
2978 G04

ADC-INL



2978 G05

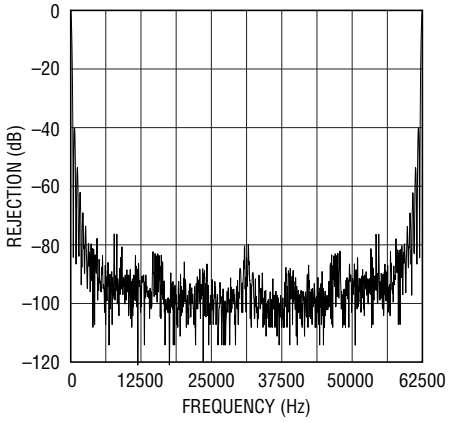
ADC-DNL



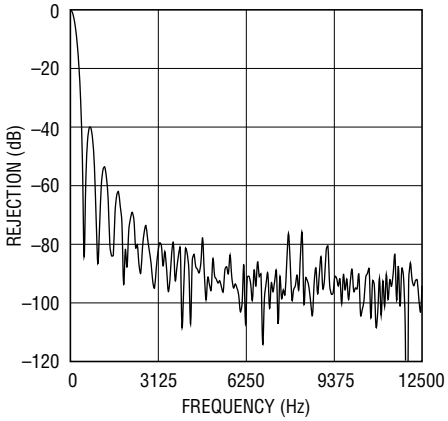
2978 G06

TYPICAL PERFORMANCE CHARACTERISTICS

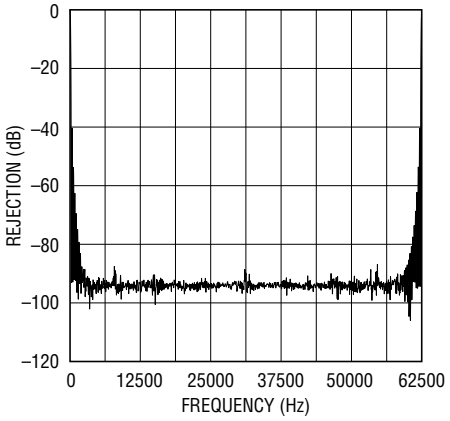
ADC Rejection vs Frequency at V_{IN}



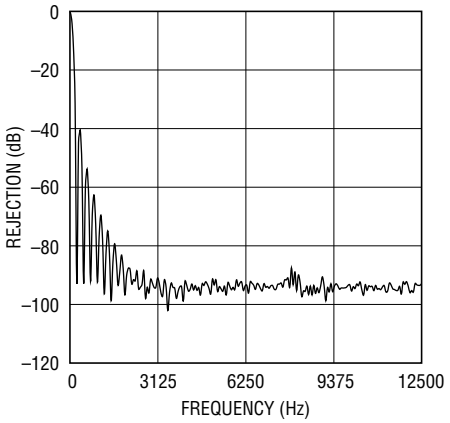
ADC Rejection vs Frequency at V_{IN} (Zoom)



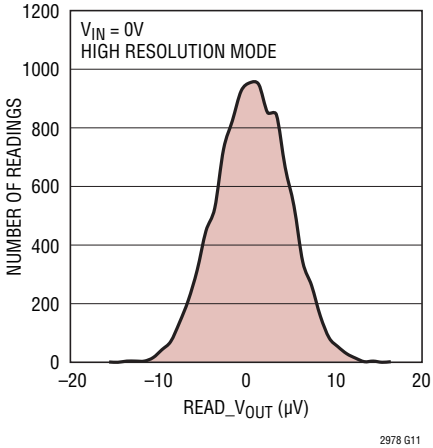
ADC Rejection vs Frequency at V_{IN} (Current Sense Mode)



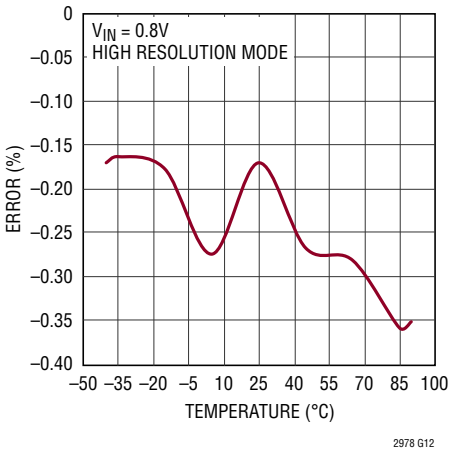
ADC Rejection vs Frequency at V_{IN} (Current Sense Mode, Zoom)



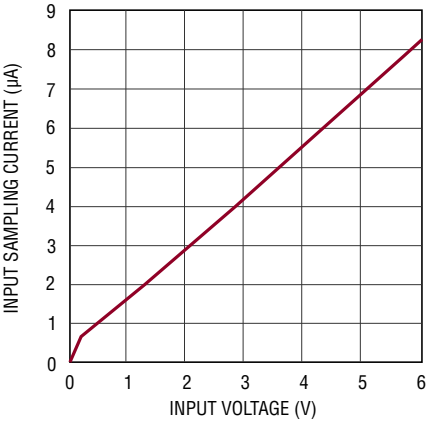
ADC Noise Histogram



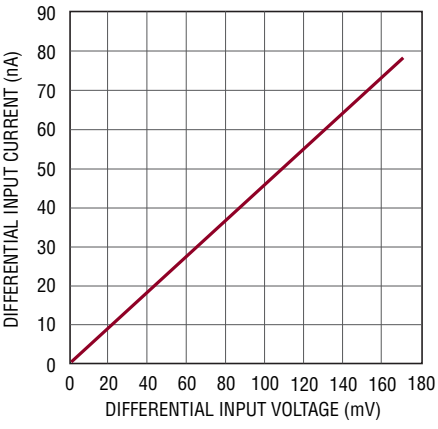
Voltage Supervisor Total Unadjusted Error vs Temperature



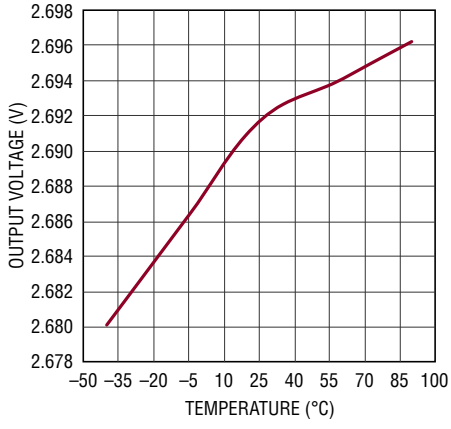
Input Sampling Current vs Differential Input Voltage



ADC High Resolution Mode Differential Input Current

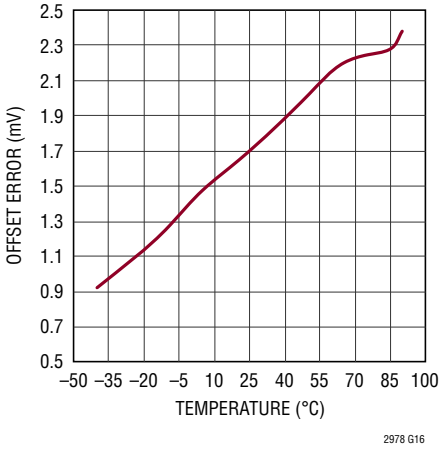


Voltage Buffered IDAC Full-Scale Output Voltage vs Temperature

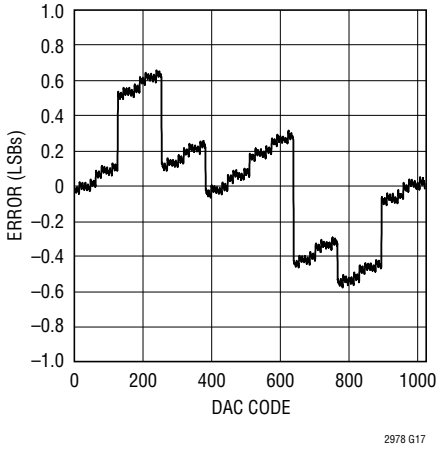


TYPICAL PERFORMANCE CHARACTERISTICS

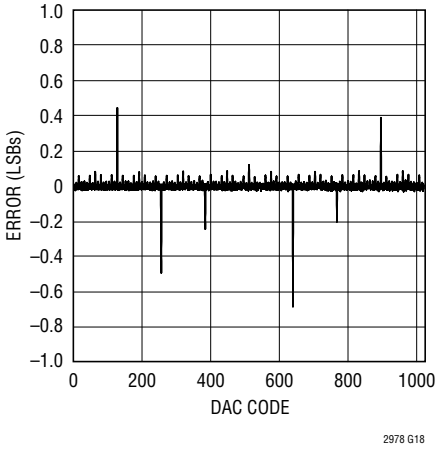
Voltage Buffered IDAC Offset Voltage vs Temperature



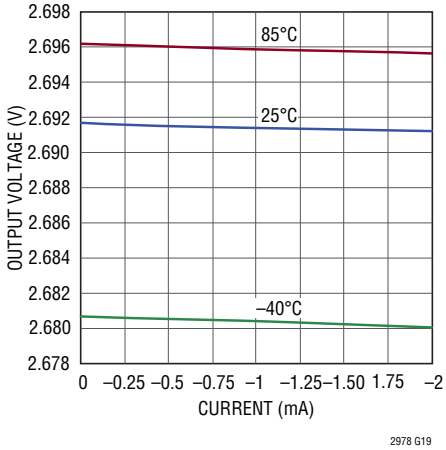
Voltage Buffered IDAC-INL



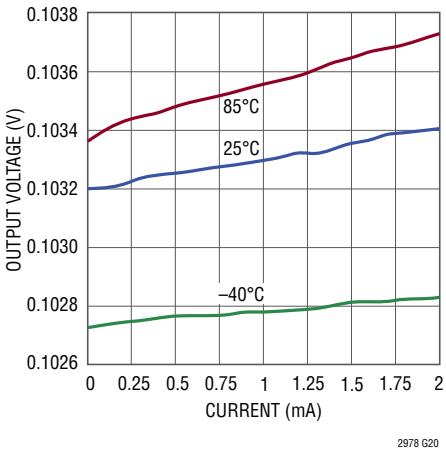
Voltage Buffered IDAC DNL



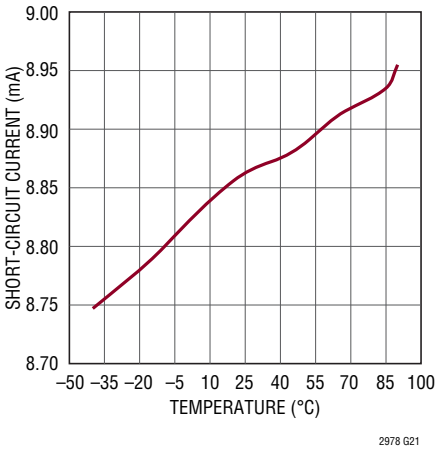
Voltage Buffered IDAC Load Regulation (Sourcing)



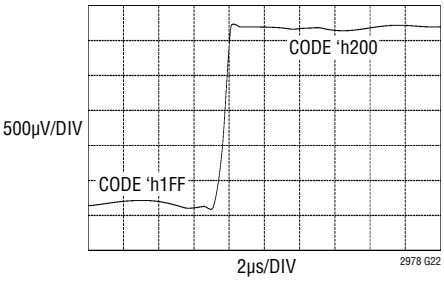
IDAC Voltage Buffer Load Regulation (Sinking)



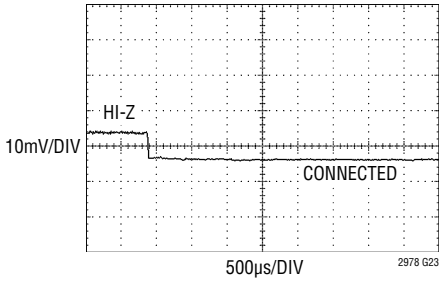
IDAC Voltage Buffer Short-Circuit Current vs Temperature



IDAC Voltage Buffer Transient Response to 1LSB DAC Code Change

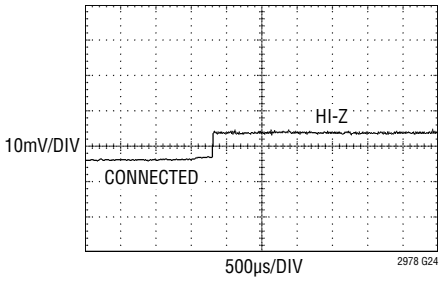


IDAC Voltage Buffer Soft Connect Transient Response when Transitioning from Hi-Z State to ON State



100k SERIES RESISTANCE ON
CODE: 'h1FF

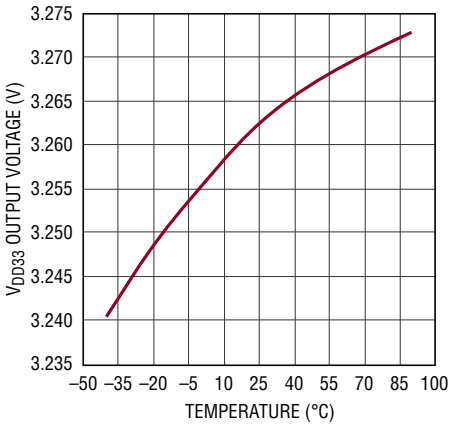
IDAC Voltage Buffer Soft Connect Transient Response when Transitioning from ON State to Hi-Z State



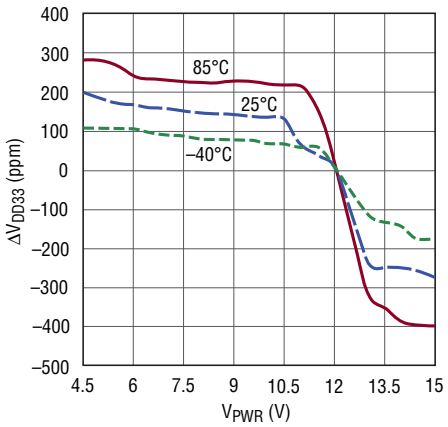
100k SERIES RESISTANCE ON
CODE: 'h1FF

TYPICAL PERFORMANCE CHARACTERISTICS

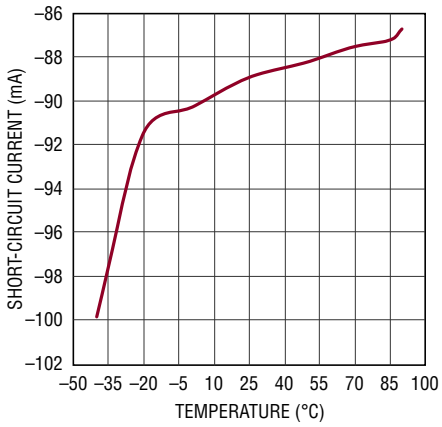
V_{DD33} Regulator Output Voltage vs Temperature



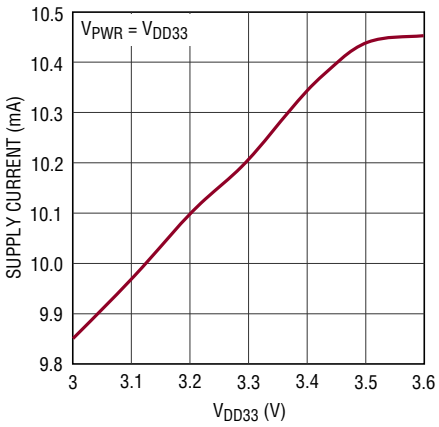
V_{DD33} Regulator Line Regulation



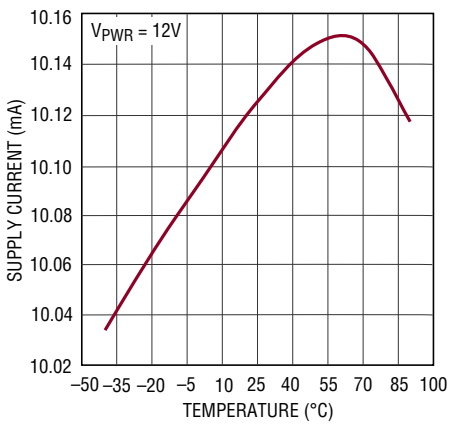
V_{DD33} Regulator Short-Circuit Current vs Temperature



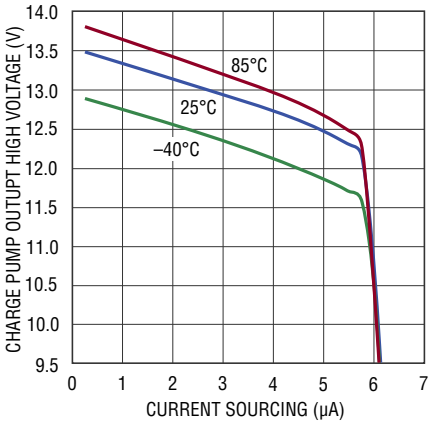
Supply Current vs Supply Voltage



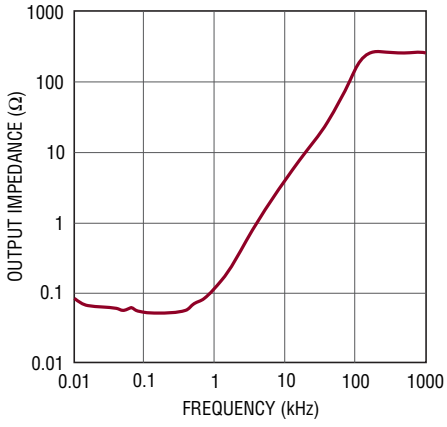
Supply Current vs Temperature



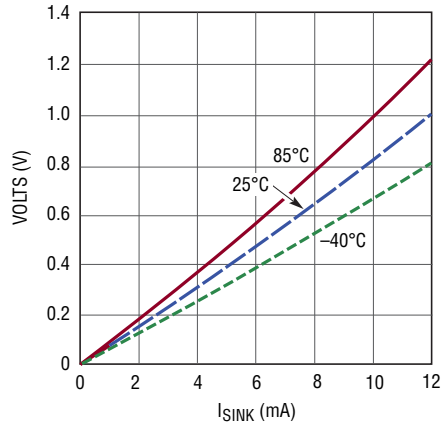
$V_{OUT\_EN[3:0]}$ and V_{IN_EN} Output High Voltage vs Load Current



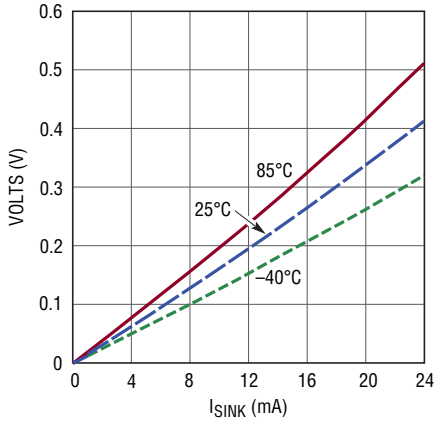
Voltage Buffered IDAC Output Impedance vs Frequency



$V_{OUT\_EN[3:0]}$ and V_{IN_EN} V_{OL} vs Current

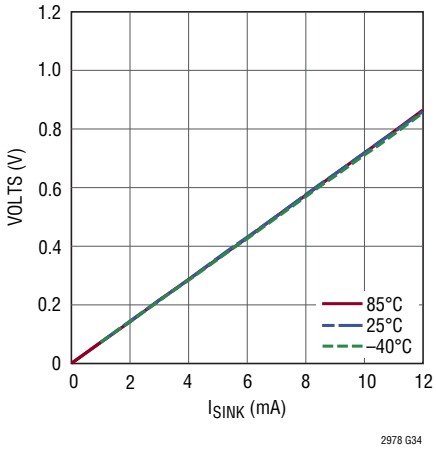


$V_{OUT\_EN[7:4]}$ V_{OL} vs Current

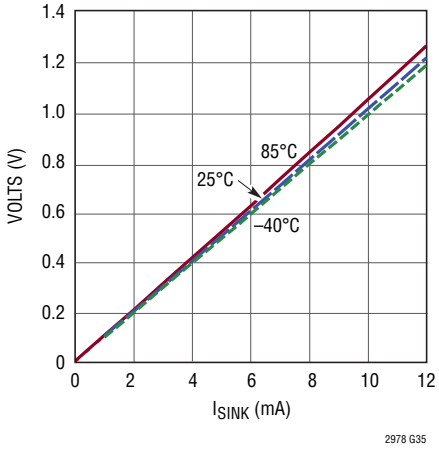


TYPICAL PERFORMANCE CHARACTERISTICS

PWRGD and FAULTBz*n* V_{OL} vs Current



ALERTB V_{OL} vs Current



PIN FUNCTIONS

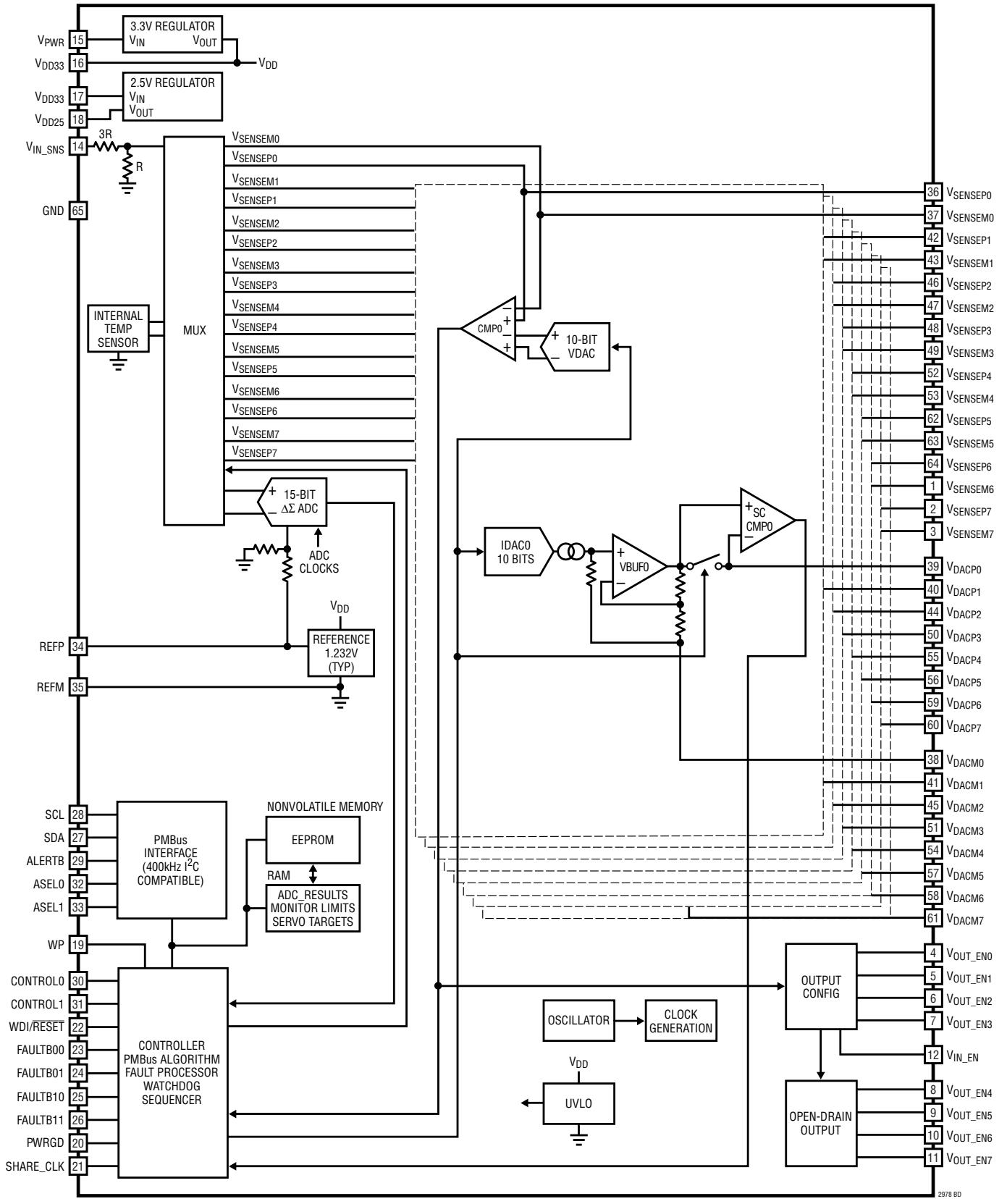
PIN NAME	PIN NUMBER	PIN TYPE	DESCRIPTION
$V_{SENSEM6}$	1*	In	DC/DC Converter Differential (–) Output Voltage-6 Sensing Pin
$V_{SENSEP7}$	2*	In	DC/DC Converter Differential (+) Output Voltage or Current-7 Sensing Pin
$V_{SENSEM7}$	3*	In	DC/DC Converter Differential (–) Output Voltage or Current-7 Sensing Pin
V_{OUT_EN0}	4	Out	DC/DC Converter Enable-0 Pin. Output High Voltage Optionally Pulled Up to 12V by 5µA
V_{OUT_EN1}	5	Out	DC/DC Converter Enable-1 Pin. Output High Voltage Optionally Pulled Up to 12V by 5µA
V_{OUT_EN2}	6	Out	DC/DC Converter Enable-2 Pin. Output High Voltage Optionally Pulled Up to 12V by 5µA
V_{OUT_EN3}	7	Out	DC/DC Converter Enable-3 Pin. Output High Voltage Optionally Pulled Up to 12V by 5µA
V_{OUT_EN4}	8	Out	DC/DC Converter Open-Drain Pull-Down Output-4
V_{OUT_EN5}	9	Out	DC/DC Converter Open-Drain Pull-Down Output-5
V_{OUT_EN6}	10	Out	DC/DC Converter Open-Drain Pull-Down Output-6
V_{OUT_EN7}	11	Out	DC/DC Converter Open-Drain Pull-Down Output-7
V_{IN_EN}	12	Out	DC/DC Converter V_{IN} ENABLE Pin. Output High Voltage Optionally Pulled Up to 12V by 5µA
DNC	13	Do Not Connect	Do Not Connect to This Pin
V_{IN_SNS}	14	In	V_{IN} SENSE Input. This Voltage is Compared Against the V_{IN} On and Off Voltage Thresholds in Order to Determine When to Enable and Disable, Respectively, the Downstream DC/DC Converters
V_{PWR}	15	In	V_{PWR} Serves as the Unregulated Power Supply Input to the Chip (4.5V to 15V). If a 4.5V to 15V Supply Voltage is Unavailable, Short V_{PWR} to V_{DD33} and Power the Chip Directly from a 3.3V Supply
V_{DD33}	16	In/Out	If Shorted to V_{PWR}, it Serves as 3.13V to 3.47V Supply Input Pin. Otherwise it is a 3.3V Internally Regulated Voltage Output (Use 100nF Decoupling Capacitor to GND)
V_{DD33}	17	In	Input for Internal 2.5V Sub-Regulator. Short This Pin to Pin 16
V_{DD25}	18	In/Out	2.5V Internally Regulated Voltage Output. Bypass to GND with a 0.1µF Capacitor
WP	19	In	Digital Input. Write-Protect Input Pin, Active High
PWRGD	20	Out	Power Good Open-Drain Output. Indicates When Outputs are Power Good. Can be Used as System Power-On Reset
SHARE_CLK	21	In/Out	Bidirectional Clock Sharing Pin. Connect a 5.49k Pull-Up Resistor to V_{DD33}
WDI/$\overline{RESET}$	22	In	Watchdog Timer Interrupt and Chip Reset Input. Connect a 10k Pull-Up Resistor to V_{DD33}. Rising Edge Resets Watchdog Counter. Holding This Pin Low for More Than t_{RESETB} Resets the Chip

PIN FUNCTIONS

FAULTB00	23	In/Out	Open-Drain Output and Digital Input. Active Low Bidirectional Fault Indicator-00. Connect a 10k Pull-Up Resistor to V_{DD33}
FAULTB01	24	In/Out	Open-Drain Output and Digital Input. Active Low Bidirectional Fault Indicator-01. Connect a 10k Pull-Up Resistor to V_{DD33}
FAULTB10	25	In/Out	Open-Drain Output and Digital Input. Active Low Bidirectional Fault Indicator-10. Connect a 10k Pull-Up Resistor to V_{DD33}
FAULTB11	26	In/Out	Open-Drain Output and Digital Input. Active Low Bidirectional Fault Indicator-11. Connect a 10k Pull-Up Resistor to V_{DD33}
SDA	27	In/Out	PMBus Bidirectional Serial Data Pin
SCL	28	In	PMBus Serial Clock Input Pin (400kHz Maximum)
ALERTB	29	Out	Open-Drain Output. Generates an Interrupt Request in a Fault/Warning Situation
CONTROL0	30	In	Control Pin 0 Input
CONTROL1	31	In	Control Pin 1 Input
ASEL0	32	In	Ternary Address Select Pin 0 Input. Connect to V_{DD33}, GND or Float to Encode 1 of 3 Logic States
ASEL1	33	In	Ternary Address Select Pin 1 Input. Connect to V_{DD33}, GND or Float to Encode 1 of 3 Logic States
REFP	34	Out	Reference Voltage Output. Needs 0.1µF Decoupling Capacitor to REFM
REFM	35	Out	Reference Return Pin. Needs 0.1µF Decoupling Capacitor to REFP.
$V_{SENSEP0}$	36*	In	DC/DC Converter Differential (+) Output Voltage-0 Sensing Pin
$V_{SENSEM0}$	37*	In	DC/DC Converter Differential (–) Output Voltage-0 Sensing Pin
V_{DACM0}	38	Out	Voltage Buffered IDAC0 Return. Connect to Channel 0 DC/DC Converter's GND Sense or Return to GND
V_{DACP0}	39	Out	Voltage Buffered IDAC0 Output
V_{DACP1}	40	Out	Voltage Buffered IDAC1 Output
V_{DACM1}	41	Out	Voltage Buffered IDAC1 Return. Connect to Channel 1 DC/DC Converter's GND Sense or Return to GND
$V_{SENSEP1}$	42*	In	DC/DC Converter Differential (+) Output Voltage or Current-1 Sensing Pins
$V_{SENSEM1}$	43*	In	DC/DC Converter Differential (–) Output Voltage or Current-1 Sensing Pins
V_{DACP2}	44	Out	Voltage Buffered IDAC2 Output
V_{DACM2}	45	Out	Voltage Buffered IDAC2 Return. Connect to Channel 2 DC/DC Converter's GND Sense or Return to GND
$V_{SENSEP2}$	46*	In	DC/DC Converter Differential (+) Output Voltage-2 Sensing Pin
$V_{SENSEM2}$	47*	In	DC/DC Converter Differential (–) Output Voltage-2 Sensing Pin
$V_{SENSEP3}$	48*	In	DC/DC Converter Differential (+) Output Voltage or Current-3 Sensing Pins
$V_{SENSEM3}$	49*	In	DC/DC Converter Differential (–) Output Voltage or Current-3 Sensing Pins
V_{DACP3}	50	Out	Voltage Buffered IDAC3 Output
V_{DACM3}	51	Out	Voltage Buffered IDAC3 Return. Connect to Channel 3 DC/DC Converter's GND Sense or Return to GND
$V_{SENSEP4}$	52*	In	DC/DC Converter Differential (+) Output Voltage-4 Sensing Pin
$V_{SENSEM4}$	53*	In	DC/DC Converter Differential (–) Output Voltage-4 Sensing Pin
V_{DACM4}	54	Out	Voltage Buffered IDAC4 Return. Connect to Channel 4 DC/DC Converter's GND Sense or Return to GND
V_{DACP4}	55	Out	Voltage Buffered IDAC4 Output
V_{DACP5}	56	Out	Voltage Buffered IDAC5 Output
V_{DACM5}	57	Out	Voltage Buffered IDAC5 Return. Connect to Channel 5 DC/DC Converter's GND Sense or Return to GND
V_{DACM6}	58	Out	Voltage Buffered IDAC6 Return. Connect to Channel 6 DC/DC Converter's GND Sense or Return to GND
V_{DACP6}	59	Out	Voltage Buffered IDAC6 Output
V_{DACP7}	60	Out	Voltage Buffered IDAC7 Output
V_{DACM7}	61	Out	Voltage Buffered IDAC7 Return. Connect to Channel 7 DC/DC Converter's GND Sense or Return to GND
$V_{SENSEP5}$	62*	In	DC/DC Converter Differential (+) Output Voltage or Current-5 Sensing Pins
$V_{SENSEM5}$	63*	In	DC/DC Converter Differential (–) Output Voltage or Current-5 Sensing Pins
$V_{SENSEP6}$	64*	In	DC/DC Converter Differential (+) Output Voltage-6 Sensing Pin
GND	65	Ground	Exposed Pad, Must be Soldered to PCB

*Any unused $V_{SENSEPn}$ or $V_{SENSEMn}$ pins must be tied to GND.

BLOCK DIAGRAM



OPERATION

OPERATION OVERVIEW

The LTC2978 is a PMBus programmable power supply controller, monitor, sequencer and voltage supervisor that can perform the following operations:

- Accept PMBus compatible programming commands.
- Provide DC/DC converter input voltage and output voltage/current read back through the PMBus interface.
- Control the output of modules that set voltage with a trim pin or modules that set the output voltage using an external resistor feedback network.
- Sequence the start-up of DC/DC converters via PMBus programming and the CONTROL input pins.
- Trim the DC/DC converter output voltage (typically in 0.1% steps), in closed-loop servo operating mode, through PMBus programming.
- Margin the DC/DC converter output voltage to PMBus programmed limits (typically ±10%).
- Allow the user to trim or margin the DC/DC converter output voltage in a manual operating mode by providing direct access to the margin DAC.
- Supervise the DC/DC converter output voltage, input voltage, and the LTC2978 die temperature for overvalue/undervalue conditions with respect to PMBus programmed limits and generate appropriate faults and warnings.
- Respond to a fault condition by either continuing operation indefinitely, latching off after a programmable de-glitch period or latching off immediately. A retry mode may be used to automatically recover from a latched-off condition.
- Stop trimming the DC/DC converter output voltage after it reached the initial margin or nominal target. Optionally allows servo to resume if target drifts outside of V_{OUT} warning limits.
- Store command register contents to EEPROM through PMBus programming.
- Restore EEPROM contents through PMBus programming or on POR.
- Report the DC/DC converter output voltage status through the PMBus interface and the power good output.
- Generate interrupt requests by asserting the ALERTB pin in response to supported PMBus faults.
- Shut down multiple DC/DC converters in response to a fault through the FAULTBz0 and FAULTBz1 pins.
- Synchronize sequencing delays or shutdown for multiple devices using the SHARE_CLK pin.
- Software and hardware write protect the command registers.
- Disable the input voltage to the supervised DC/DC converters in response to output voltage OV and UV faults.
- Log telemetry and status data to EEPROM in response to a faulted-off condition
- Supervise an external microcontroller's activity for a stalled condition with a programmable watchdog timer and reset it if necessary.
- Prevent a DC/DC converter from re-entering the ON state after a power cycle until a programmable interval (MFR_RESTART_DELAY) has elapsed and its output has decayed below a programmable threshold voltage (MFR_VOUT_DISCHARGE_THRESHOLD).
- Record minimum and maximum observed values of input voltage, output voltages and temperature.

OPERATION

PMBus SERIAL DIGITAL INTERFACE

The LTC2978 communicates with a host (master) using the standard PMBus serial bus interface. The Timing Diagram shows the timing relationship of the signals on the bus. The two bus lines, SDA and SCL, must be high when the bus is not in use. External pull-up resistors or current sources are required on these lines.

The LTC2978 is a slave device. The master can communicate with the LTC2978 using the following formats:

- Master transmitter, slave receiver
- Master receiver, slave transmitter

The following SMBus protocols are supported:

- Write Byte, Write Word, Send Byte
- Read Byte, Read Word, Block Read
- Alert Response Address

Figures 1-10 illustrate the aforementioned SMBus protocols. All transactions support PEC (parity error check) and GCP (group command protocol). The Block Read supports 256 bytes of returned data. For this reason, the PMBus timeout may be extended using the Mfr_config_all_longer_pmbus_timeout setting.

The LTC2978 will not acknowledge any PMBus command if it is still busy with a STORE_USER_ALL, RESTORE_USER_ALL, MFR_CONFIG or if fault log data is being written to the EEPROM. Status_word_busy will also be set.

Slave Address

The LTC2978 can be configured to respond to one of nine addresses for a given MFR_I2C_BASE_ADDRESS value (the factory default value for this register is 7'h5C). In addition, the LTC2978 will always respond to its global address and the PMBus Alert Response address regardless of the state of the address select pins.

By connecting each of the address inputs to V_{DD33}, GND, or by floating them, the user determines the slave address as shown in Table 1.

Table 1. LTC2978 Address Look-Up Table

DESCRIPTION	HEX DEVICE ADDRESS		BINARY DEVICE ADDRESS								ADDRESS PINS	
	7'h	8'h	6	5	4	3	2	1	0	R/W	ASEL1	ASEL0
Alert Response	0C	19	0	0	0	1	1	0	0	1	X	X
Global	5B	B6	1	0	1	1	0	1	1	0	X	X
0*	5C	B8	1	0	1	1	1	0	0	0	L	L
1	5D	BA	1	0	1	1	1	0	1	0	L	NC
2	5E	BC	1	0	1	1	1	1	0	0	L	H
3	5F	BE	1	0	1	1	1	1	1	0	NC	L
4	60	C0	1	1	0	0	0	0	0	0	NC	NC
5	61	C2	1	1	0	0	0	0	1	0	NC	H
6	62	C4	1	1	0	0	0	1	0	0	H	L
7	63	C6	1	1	0	0	0	1	1	0	H	NC
8	64	C8	1	1	0	0	1	0	0	0	H	H

H = Tie to V_{DD33}, NC = No Connect, Open or Float, L = Tie to GND, X = Don't Care
*MFR_I2C_BASE_ADDRESS = 7'h5C (Factory Default)

OPERATION

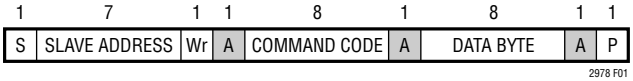


Figure 1. Write Byte Protocol

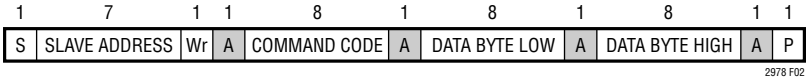


Figure 2. Write Word Protocol

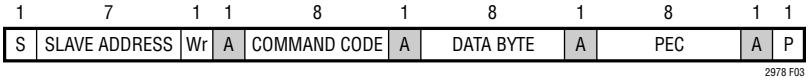


Figure 3. Write Byte Protocol with PEC

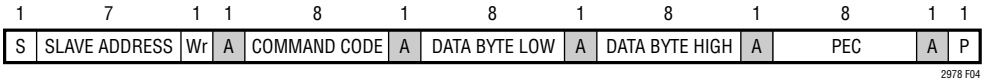


Figure 4. Write Word Protocol with PEC

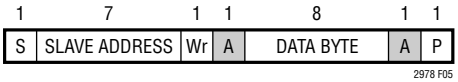


Figure 5. Send Byte Protocol

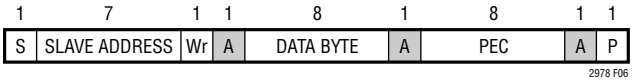


Figure 6. Send Byte Protocol with PEC

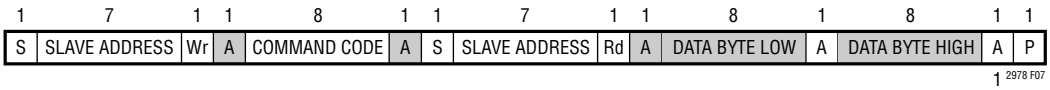


Figure 7. Read Word Protocol

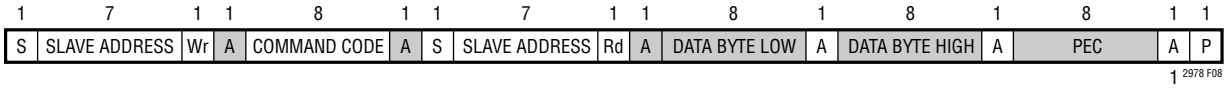


Figure 8. Read Word Protocol with PEC

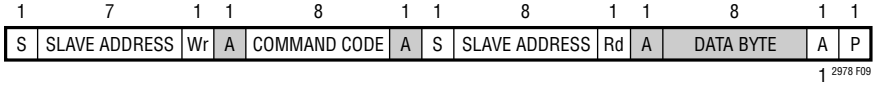


Figure 9. Read Byte Protocol

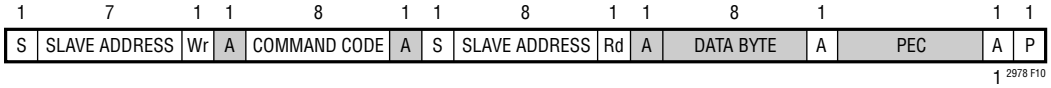


Figure 10. Read Byte Protocol with PEC

OPERATION

REGISTER COMMAND SET

Summary

COMMAND FUNCTION	DESCRIPTION	R/W	DATA LENGTH (BITS)	COMMAND BYTE VALUE	NV MEMORY TYPE	DEFAULT VALUE	PAGED ?
PAGE		R/W	8	‘h00		‘h00	N
OPERATION	Operating mode control.	R/W	8	‘h01	EEPROM	‘h00	Y
ON_OFF_CONFIG	CONTROL pin and PMBus bus on/off command setting.	R/W	8	‘h02	EEPROM	‘h12	Y
CLEAR_FAULTS	CLEAR_FAULTS is used to clear any fault bits that have been set.	W	0	‘h03		NA	Y
WRITE_PROTECT	Provides protection against accidental changes.	R/W	8	‘h10	EEPROM	‘h00	N
STORE_USER_ALL	Store entire operating memory to EEPROM.	W	0	‘h15		NA	N
RESTORE_USER_ALL	Restore entire operating memory from EEPROM.	W	0	‘h16		NA	N
CAPABILITY	The CAPABILITY command provides a way for a host system to determine the capabilities of the PMBus device.	R	8	‘h19	ROM	‘hE0	N
VOUT_MODE	Output voltage format control.	R	8	‘h20	ROM	‘h13	Y
VOUT_COMMAND	Servo DC/DC converter output voltage value setting.	R/W	16	‘h21	EEPROM	‘h2000	Y
VOUT_MAX	The VOUT_MAX command sets an upper limit on the output voltage, in volts, the unit can command regardless of any other commands or combinations.	R/W	16	‘h24	EEPROM	‘h8000	Y
VOUT_MARGIN_HIGH	Margin high DC/DC converter output voltage limit setting.	R/W	16	‘h25	EEPROM	‘h219A	Y
VOUT_MARGIN_LOW	Margin low DC/DC converter output voltage limit setting.	R/W	16	‘h26	EEPROM	‘h1E66	Y
VIN_ON	The VIN_ON command sets the input voltage, in volts, at which the unit should start power conversion.	R/W	16	‘h35	EEPROM	‘hD280	N
VIN_OFF	The VIN_OFF command sets the input voltage, in volts, at which the unit should stop power conversion.	R/W	16	‘h36	EEPROM	‘hD240	N
VOUT_OV_FAULT_LIMIT	Overvoltage DC/DC converter fault limit setting.	R/W	16	‘h40	EEPROM	‘h2333	Y
VOUT_OV_FAULT_RESPONSE	The VOUT_OV_FAULT_RESPONSE command instructs the device on what action to take in response to an output overvoltage fault.	R/W	8	‘h41	EEPROM	‘h80	Y
VOUT_OV_WARN_LIMIT	Overvoltage DC/DC converter warning limit setting.	R/W	16	‘h42	EEPROM	‘h2266	Y
VOUT_UV_WARN_LIMIT	Undervoltage DC/DC converter warning limit setting.	R/W	16	‘h43	EEPROM	‘h1D9A	Y

OPERATION

Summary

COMMAND FUNCTION	DESCRIPTION	R/W	DATA LENGTH (BITS)	COMMAND BYTE VALUE	NV MEMORY TYPE	DEFAULT VALUE	PAGED ?
VOUT_UV_FAULT_LIMIT	Undervoltage DC/DC converter fault limit setting. This limit is also used to determine if Ton_max_fault has been met and the unit is on.	R/W	16	‘h44	EEPROM	‘h1CCD	Y
VOUT_UV_FAULT_RESPONSE	The VOUT_UV_FAULT_RESPONSE command instructs the device on what action to take in response to an undervoltage fault.	R/W	8	‘h45	EEPROM	‘h7F	Y
OT_FAULT_LIMIT	Overtemperature fault limit setting.	R/W	16	‘h4F	EEPROM	‘hEAA8	N
OT_FAULT_RESPONSE	The OT_FAULT_RESPONSE command instructs the device on what action to take in response to an overtemperature fault.	R/W	8	‘h50	EEPROM	‘hB8	N
OT_WARN_LIMIT	Overtemperature warning limit setting.	R/W	16	‘h51	EEPROM	‘hEA58	N
UT_WARN_LIMIT	Undertemperature warn limit setting.	R/W	16	‘h52	EEPROM	‘h8000	N
UT_FAULT_LIMIT	Undertemperature fault limit setting.	R/W	16	‘h53	EEPROM	‘hCD80	N
UT_FAULT_RESPONSE	The UT_FAULT_RESPONSE command instructs the device on what action to take in response to an undertemperature fault.	R/W	8	‘h54	EEPROM	‘hB8	N
VIN_OV_FAULT_LIMIT	Input supply overvoltage fault limit setting.	R/W	16	‘h55	EEPROM	‘hD3C0	N
VIN_OV_FAULT_RESPONSE	The VIN_OV_FAULT_RESPONSE command instructs the device on what action to take in response to an input overvoltage fault.	R/W	8	‘h56	EEPROM	‘h80	N
VIN_OV_WARN_LIMIT	Overvoltage input supply warning limit setting.	R/W	16	‘h57	EEPROM	‘hD380	N
VIN_UV_WARN_LIMIT	Undervoltage input supply warning limit setting.	R/W	16	‘h58	EEPROM	‘h8000	N
VIN_UV_FAULT_LIMIT	Undervoltage input supply fault limit setting.	R/W	16	‘h59	EEPROM	‘h8000	N
VIN_UV_FAULT_RESPONSE	The VIN_UV_FAULT_RESPONSE command instructs the device on what action to take in response to an input undervoltage fault.	R/W	8	‘h5A	EEPROM	‘h00	N
POWER_GOOD_ON	Output voltage at or above which a power good should be asserted.	R/W	16	‘h5E	EEPROM	‘h1EB8	Y
POWER_GOOD_OFF	Output voltage at or below which a power good should be deasserted.	R/W	16	‘h5F	EEPROM	‘h1E14	Y
TON_DELAY	Time, in ms, from CONTROL and/or Operation on to V_{OUT_EN} on.	R/W	16	‘h60	EEPROM	‘hBA00	Y
TON_RISE	Time, in ms, from when the output starts to rise until the LTC2978 optionally soft-connects its voltage-buffered current DAC and begins to servo the output voltage to the desired value.	R/W	16	‘h61	EEPROM	‘hD280	Y
TON_MAX_FAULT_LIMIT	Maximum time, in ms, from V_{OUT_EN} on assertion that an UV condition will be tolerated before a TON_MAX_FAULT condition results.	R/W	16	‘h62	EEPROM	‘hD3C0	Y
TON_MAX_FAULT_RESPONSE	Specifies response to a TON_MAX_FAULT event.	R/W	8	‘h63	EEPROM	‘hB8	Y

OPERATION

Summary

COMMAND FUNCTION	DESCRIPTION	R/W	DATA LENGTH (BITS)	COMMAND BYTE VALUE	NV MEMORY TYPE	DEFAULT VALUE	PAGED ?
TOFF_DELAY	Time, in ms, from CONTROL and/or Operation off to VOUT_EN off.	R/W	16	‘h64	EEPROM	‘hBA00	Y
STATUS_BYTE	Fault status reporting.	R	8	‘h78		NA	Y
STATUS_WORD	The STATUS_WORD command returns two bytes of information with a summary of the unit’s fault condition.	R	16	‘h79		NA	Y
STATUS_VOUT	Voltage fault status reporting.	R	8	‘h7A		NA	Y
STATUS_INPUT	The STATUS_INPUT command returns one byte with status on V_{IN_SNS}.	R	8	‘h7C		NA	N
STATUS_TEMPERATURE	The STATUS_TEMPERATURE command returns one byte with status information on temperature.	R	8	‘h7D		NA	N
STATUS_CML	The STATUS_CML command returns one byte with status information on communication and memory.	R	8	‘h7E		NA	N
STATUS_MFR_SPECIFIC	The STATUS_MFR_SPECIFIC command returns one byte with the manufacturer specific status information.	R	8	‘h80		NA	Y
READ_VIN	Input supply voltage read back.	R	16	‘h88		NA	N
READ_VOUT	DC/DC converter output voltage read back.	R	16	‘h8B		NA	Y
READ_TEMPERATURE_1	Internal junction temperature read back.	R	16	‘h8D		NA	N
PMBUS_REVISION	Read the supported PMBus revision (1.1).	R	8	‘h98	ROM	‘h11	N
MFR_CONFIG	Manufacturer configuration bits that are channel specific.	R/W	16	‘hD0	EEPROM	‘h0080	Y
MFR_CONFIG_ALL	Manufacturer configuration bits that are common to all pages.	R/W	8	‘hD1	EEPROM	‘h7B	N
MFR_FAULTBz0_PROPAGATE	Manufacturer configuration that determines which channel faults are propagated to FAULTBz0 where z = 0 for channels 0-3, and z=1 for channels 4-7.	R/W	8	‘hD2	EEPROM	‘h00	Y
MFR_FAULTBz1_PROPAGATE	Manufacturer configuration that determines which channel faults are propagated to FAULTBz1.	R/W	8	‘hD3	EEPROM	‘h00	Y
MFR_PWRGD_EN	Maps PWRGD status to the PWRGD pin.	R/W	16	‘hD4	EEPROM	‘h0000	N
MFR_FAULTB00_RESPONSE	Determines response to FAULTB00 pin being asserted low.	R/W	8	‘hD5	EEPROM	‘h00	N
MFR_FAULTB01_RESPONSE	Determines response to FAULTB01 pin being asserted low.	R/W	8	‘hD6	EEPROM	‘h00	N
MFR_FAULTB10_RESPONSE	Determines response to FAULTB10 pin being asserted low.	R/W	8	‘hD7	EEPROM	‘h00	N
MFR_FAULTB11_RESPONSE	Determines response to FAULTB11 pin being asserted low.	R/W	8	‘hD8	EEPROM	‘h00	N
MFR_VINEN_OV_FAULT_RESPONSE	Determines the response of the VIN_EN pin to a VOUT_OV_FAULT	R/W	8	‘hD9	EEPROM	‘h00	N

OPERATION

Summary

COMMAND FUNCTION	DESCRIPTION	R/W	DATA LENGTH (BITS)	COMMAND BYTE VALUE	NV MEMORY TYPE	DEFAULT VALUE	PAGED ?
MFR_VINEN_UV_FAULT_RESPONSE	Determines the response of the VIN_EN pin to a VOUT_UV_FAULT	R/W	8	‘hDA	EEPROM	‘h00	N
MFR_RETRY_DELAY	Sets retry interval during retry mode.	R/W	16	‘hDB	EEPROM	‘hF320	N
MFR_RESTART_DELAY	Sets delay from actual CONTROL active edge to virtual CONTROL active edge.	R/W	16	‘hDC	EEPROM	‘hFB20	N
MFR_VOUT_PEAK	Returns the maximum measured value of V_{OUT}.	R	16	‘hDD		NA	Y
MFR_VIN_PEAK	Returns the maximum measured value of V_{IN_SNS}.	R	16	‘hDE		NA	N
MFR_TEMPERATURE_PEAK	Returns the maximum measured value of temperature.	R	16	‘hDF		NA	N
MFR_DAC	Manufacturer register that contains the code of the 10-bit voltage-buffered current DAC.	R/W	16	‘hE0	EEPROM	‘h0000	Y
MFR_POWERGOOD_ASSERTION_DELAY	Determines power good output assertion delay.	R/W	16	‘hE1	EEPROM	‘hEB20	N
MFR_WATCHDOG_T_FIRST	First watchdog timer interval.	R/W	16	‘hE2	EEPROM	‘h8000	N
MFR_WATCHDOG_T	Watchdog timer interval.	R/W	16	‘hE3	EEPROM	‘h8000	N
MFR_PAGE_FF_MASK	Selects which channels respond to global page commands.	R/W	8	‘hE4	EEPROM	‘hFF	N
MFR_PADS	Returns values detected and driven onto digital I/O pads.	R	16	‘hE5		N/A	N
MFR_I2C_BASE_ADDRESS	This register determines the base value of the I^2C address byte.	R/W	8	‘hE6	EEPROM	‘h5C	N
MFR_SPECIAL_ID	This register contains the manufacturer code for identifying the LTC2978.	R	16	‘hE7	EEPROM	‘h0121	N
MFR_SPECIAL_LOT	These registers contain customer dependent codes that identify the factory programmed user configuration stored in EEPROM.	R/W	8	‘hE8	EEPROM	Contact the Factory	Y
MFR_VOUT_DISCHARGE_THRESHOLD	Coefficient used to multiply VOUT_COMMAND in order to determine VOUT OFF threshold voltage.	R/W	16	‘hE9	EEPROM	‘hC200	Y
MFR_FAULT_LOG_STORE	Command a transfer of the fault log from RAM to EEPROM. This causes the part to behave as if a channel has faulted off.	W	0	‘hEA		NA	N
MFR_FAULT_LOG_RESTORE	Command a transfer of the fault log previously stored in EEPROM back to RAM.	W	0	‘hEB		NA	N
MFR_FAULT_LOG_CLEAR	Initialize the EEPROM block reserved for fault logging and clear any previous fault logging locks.	W	0	‘hEC		NA	N
MFR_FAULT_LOG_STATUS	This command returns one byte with status information on fault logging.	R	8	‘hED	EEPROM	NA	N
MFR_FAULT_LOG	Fault log. Accessed using a block read. Returns data in the form last in first out.	R	2048	‘hEE	EEPROM	NA	N

OPERATION

Summary

COMMAND FUNCTION	DESCRIPTION	R/W	DATA LENGTH (BITS)	COMMAND BYTE VALUE	NV MEMORY TYPE	DEFAULT VALUE	PAGED ?
MFR_COMMON	Contains manufacturer status bits that are common across multiple LTC chips.	R	8	‘hEF		NA	N
MFR_SPARE_0	Scratchpad register.	R/W	16	‘hF7	EEPROM	‘h0000	N
MFR_SPARE_2	Paged scratchpad register.	R/W	16	‘hF9	EEPROM	‘h0000	Y
MFR_VOUT_MIN	Returns the minimum measured value of VOUT.	R	16	‘hFB		NA	Y
MFR_VIN_MIN	Returns the minimum measured value of V_{IN_SNS}.	R	16	‘hFC		NA	N
MFR_TEMPERATURE_MIN	Returns the minimum measured junction temperature value.	R	16	‘hFD		NA	N

DETAILED PMBus COMMAND REGISTER DESCRIPTIONS

PAGE

The PAGE command provides the ability to configure, control and monitor multiple outputs on one unit. Setting PAGE = ‘hFF allows PMBus commands that support global page programming to be written simultaneously. The only commands that support PAGE = ‘hFF are OPERATION and ON_OFF_CONFIG. See MFR_PAGE_FF_MASK for additional options. Reading any PMBus register with PAGE = ‘hFF returns unpredictable data and will trigger a CML fault.

PAGE Data Contents

BIT(S)	SYMBOL	PURPOSE
b[7:0]	Page	Page operation. ‘h00: All PMBus commands address channel/page 0. ‘h01: All PMBus commands address channel/page 1. • • • ‘h07: All PMBus commands address channel/page 7. ‘hXX: All nonspecified values reserved. ‘hFF: PMBus commands that support this global PAGE write mode will be written simultaneously.

OPERATION

OPERATION

The OPERATION command is used to turn the unit on and off in conjunction with the CONTROL*n* pin and ON_OFF_CONFIG. This command register responds to the global page command. The contents and functions of the data byte are shown in the following tables.

OPERATION Data Contents When On_Off_Config_Use_PMBus Enables Operation_Control

SYMBOL	Action	Operation_control[1:0]	Operation_margin[1:0]	Operation_fault[1:0]	Reserved (read only)
BITS		b[7:6]	b[5:4]	b[3:2]	b[1:0]
FUNCTION	Turn off immediately	00	XX	XX	00
	Turn on	10	00	XX	00
	Margin Low (Ignore Faults and Warnings)	10	01	01	00
	Margin Low	10	01	10	00
	Margin High (Ignore Faults and Warnings	10	10	01	00
	Margin High	10	10	10	00
	Sequence off and margin to nominal	01	00	XX	00
	Sequence off and Margin Low (Ignore Faults and Warnings)	01	01	01	00
	Sequence off and Margin Low	01	01	10	00
	Sequence off and Margin High (Ignore Faults and Warnings)	01	10	01	00
	Sequence off and Margin High	01	10	10	00
	Reserved	All remaining combinations			

OPERATION Data Contents When On_Off_Config is Configured Such That OPERATION Command is Not Used to Command Channel On or Off

SYMBOL	Action	Operation_control[1:0]	Operation_margin[1:0]	Operation_fault[1:0]	Reserved (read only)
BITS		b[7:6]	b[5:4]	b[3:2]	b[1:0]
FUNCTION	Output at Nominal	00, 01 or 10	00	XX	00
	Margin Low (Ignore faults and Warnings)	00, 01 or 10	01	01	00
	Margin Low	00, 01 or 10	01	10	00
	Margin High (Ignore Faults and Warnings	00, 01 or 10	10	01	00
	Margin High	00, 01 or 10	10	10	00
	Reserved	All remaining combinations			

OPERATION

ON_OFF_CONFIG

The ON_OFF_CONFIG command configures the combination of CONTROL*n* pin input and PMBus bus commands needed to turn the LTC2978 on/off, including the power-on behavior, as shown in the following table. This command register responds to the global page command.

ON_OFF_CONFIG Data Contents

BITS(S)	SYMBOL	OPERATION
b[7:5]	Reserved	Don't care. Always returns 0.
b[4]	On_off_config_controlled_on	Control default autonomous power-up operation. 0: Unit powers up regardless of the CONTROL*n* pin. Unit always powers up with sequencing. To turn unit on without sequencing, set TON_DELAY = 0. 1: Unit does not power up unless commanded by the CONTROL*n* pin and/or the OPERATION command on the serial bus. If On_off_config[3:2] = 00, the unit never powers up.
b[3]	On_off_config_use_pmbus	Controls how the unit responds to commands received via the serial bus. 0: Unit ignores the Operation_control[1:0]. 1: Unit responds to Operation_control[1:0]. Depending on On_off_config_use_control, the unit may also require the CONTROL*n* pin to be asserted for the unit to start.
b[2]	On_off_config_use_control	Controls how unit responds to the CONTROL*n* pin. 0: Unit ignores the CONTROL*n* pin. 1: Unit requires the CONTROL*n* pin to be asserted to start the unit. Depending on On_off_config_use_PMBus the OPERATION command may also be required to instruct the device to start.
b[1]	Reserved	Not supported. Always returns 1.
b[0]	On_off_config_control_fast_off	CONTROL*n* pin turn off action when commanding the unit to turn off 0: Use the programmed TOFF_DELAY. 1: Turn off the output and stop transferring energy as quickly as possible. The device does not sink current in order to decrease the output voltage fall time.

OPERATION

CLEAR_FAULTS

The CLEAR_FAULTS command is used to clear any status faults that have been set. This command clears all bits in all unpaged status registers, and the paged status registers selected by the current PAGE setting. At the same time, the device negates (clears, releases) its contribution to ALERTB.

The CLEAR_FAULTS command does not cause a unit that has latched off for a fault condition to restart.

If the fault condition is present after the fault status is cleared, the fault status bit shall be set again and the host notified by the usual means.

Note: this command register does not respond to the global page command.

WRITE_PROTECT

The WRITE_PROTECT command provides protection against accidental programming of the LTC2978 command registers. All supported commands may have their parameters read, regardless of the WRITE_PROTECT setting.

WRITE_PROTECT Data Contents

BITS(S)	SYMBOL	OPERATION
b[7:0]	Write_protect[7:0]	8'b1000_0000: Disable all writes except to the WRITE_PROTECT, PAGE, and STORE_USER_ALL commands. 8'b0100_0000: Disable all writes except to the WRITE_PROTECT, PAGE, STORE_USER_ALL, OPERATION, MFR_PAGE_FF_MASK, and CLEAR_FAULTS. 8'b0000_0000: Enable writes to all commands. 8'bxxxx_xxxx: All other values reserved.

STORE_USER_ALL and RESTORE_USER_ALL

STORE_USER_ALL, RESTORE_USER_ALL commands provide access to user nonvolatile EEPROM memory. Once a command is stored in EEPROM, it will be restored with explicit restore command or when the part emerges from power-on reset after power is applied. While either of these commands is being processed, the device will NACK I^2C writes.

STORE_USER_ALL. No Data Contents. Accessing this command will store all operating memory commands with a corresponding EEPROM memory location. It is recommended that this command not be executed while a unit is enabled since all monitoring is suspended while the operating memory is transferred to EEPROM.

RESTORE_USER_ALL. No Data Contents. Accessing this command will restore all commands from EEPROM Memory. It is recommend that this command not be executed while a unit is enabled since all monitoring is suspended while the EEPROM is transferred to operating memory, and intermediate values from EEPROM may not be compatible with the values initially stored in operating memory.

CAPABILITY

The CAPABILITY command provides a way for a host system to determine some key capabilities of the LTC2978. This one byte command is read only.

CAPABILITY Data Contents

BITS(S)	SYMBOL	OPERATION
b[7]	Capability_pec	Hard coded to 1 indicating Packet Error Checking is supported. Reading the Mfr_config_all_pec_en bit will indicate whether PEC is currently required.
b[6]	Capability_scl_max	Hard coded to 1 indicating the maximum supported bus speed is 400kHz.
b[5]	Capability_smb_alert	Hard coded to 1 indicating this device does have an ALERTB pin and does support the SMBus Alert Response Protocol.
b[4:0]	Reserved	X: Always returns 0.

OPERATION

VOUT_MODE

The data byte for the VOUT_MODE command is 8 bits that consists of a three bit format and a five bit exponent. The three bit format specifies PMBus linear mode for all output voltage related commands. The five bit exponent provides the exponent for the mantissa specified in the data word. The LTC2978 device sets the format at the time of manufacture. The five bit exponent is read only and is set to a value of –13 decimal.

Output voltage related commands are calculated as follows except for odd numbered channels configured to measure current:

$$\text{Voltage} = V[15:0] \bullet 2^{N}$$

where Voltage is the parameter of interest in volts.

V is a 16-bit unsigned binary integer for all voltages, (e.g. Margin_high[15:0]);

N = Vout_mode_exponent, is a 5-bit two's complementary binary integer with a value hardwired to –13 decimal.

Vout_mode_parameter is read only.

Vout_mode_type is read only.

VOUT_MODE Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:5]	Vout_mode_type	Reports linear mode. Hard wired to 3'b000.
b[4:0]	Vout_mode_parameter	Linear mode exponent. 5-bit two's complement integer. Hardwired to 'h13 (–13 decimal).

Output Voltage Related Commands

VOUT_COMMAND, VOUT_MAX, VOUT_MARGIN_HIGH, VOUT_MARGIN_LOW, VOUT_OV_FAULT_LIMIT, VOUT_OV_WARN_LIMIT, VOUT_UV_WARN_LIMIT, VOUT_UV_FAULT_LIMIT, POWER_GOOD_ON and POWER_GOOD_OFF

These commands use the same format and provide various servo, margining, and supervising limits for a channel's output voltage. When odd channels are configured to measure current, the OV_WARN_LIMIT, UV_WARN_LIMIT, OV_FAULT_LIMIT and UV_FAULT_LIMIT commands are not supported.

Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:0]	Vout_command[15:0], Vout_max[15:0], Vout_margin_high[15:0], Vout_margin_low[15:0], Vout_ov_fault_limit[15:0], Vout_ov_warn_limit[15:0], Vout_uv_warn_limit[15:0], Vout_uv_fault_limit[15:0], Power_good_on[15:0], Power_good_off[15:0]	These commands relate to output voltage. The data uses the linear mode format as defined by VOUT_MODE: $V(\text{Symbol}) = Y \bullet 2^{N}$ where Y = b[15:0] is an unsigned integer and N = Vout_mode_ parameter is a 5-bit two's complement exponent that's hardwired to –13 decimal. Units: V

OPERATION

Input Voltage Related Commands

VIN_ON, VIN_OFF, VIN_OV_FAULT_LIMIT, VIN_OV_WARN_LIMIT, VIN_UV_WARN_LIMIT and VIN_UV_FAULT_LIMIT

These commands use the same format and provide voltage supervising limits for VIN.

Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:0]	Vin_on[15:0], Vin_off[15:0], Vin_ov_fault_limit[15:0], Vin_ov_warn_limit[15:0], Vin_uv_warn_limit[15:0], Vin_uv_fault_limit[15:0]	These commands relate to input voltage. The data uses the linear format: V(Symbol) = Y • 2^N where N = b[15:11] is a 5-bit two's complement integer and Y = b[10:0] is an 11-bit two's complement integer Units: V.

Temperature Related Commands

OT_FAULT_LIMIT, OT_WARN_LIMIT, UT_WARN_LIMIT and UT_FAULT_LIMIT

These commands provide supervising limits for temperature.

Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:0]	Ot_fault_limit[15:0], Ot_warn_limit[15:0], Ut_warn_limit[15:0], Ut_fault_limit[15:0]	The data uses the linear format: T(Symbol) = Y • 2^N where N = b[15:11] is a 5-bit two's complement integer and Y = b[10:0] is an 11-bit two's complement integer Units: °C.

Timer Limits

TON_DELAY, TON_RISE, TON_MAX_FAULT_LIMIT and TOFF_DELAY

These commands share the same format and provide sequencing and timer fault and warning delays in ms.

TON_DELAY is the amount time in ms that elapses after the channel has been allowed on (usually due to CONTROL*n* pin or OPERATION command) until the channel enables the power supply. This delay is counted using SHARE_CLK only.

TON_RISE is the amount of time in ms that elapses after the power supply has been enabled until the LTC2978's voltage buffered current DAC soft connects and servo's the output voltage to the desired level if Mfr_dac_mode = 2'b00. This delay is counted using SHARE_CLK only.

TON_MAX_FAULT_LIMIT is the maximum amount of time that can elapse after the power supply has been enabled until the LTC2978 unmasks the VOUT_UV_FAULT_LIMIT threshold. (Note that a value of zero means there is no limit to how long the power supply can attempt to bring up its output voltage.) This delay is counted using SHARE_CLK only.

TOFF_DELAY is the amount of time that elapses after the CONTROL*n* pin and/or OPERATION command is deasserted until the channel is disabled (soft-off). This delay is counted using SHARE_CLK if available, otherwise the internal oscillator is used.

Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:0]	Ton_delay[15:0], Ton_rise[15:0], Ton_max_fault_limit[15:0], Toff_delay[15:0],	The data uses the linear format: T(Symbol) = Y • 2^N Where N = b[15:11] is a 5-bit two's complement integer and Y = b[10:0] is an 11-bit two's complement integer The internal timers operate on a 10µs internal clock. The SHARE_CLK pin may be used to synchronize the 10µs timer. Delays are rounded to the nearest 10µs Units: ms. Max value: 655ms

OPERATION

Fault Response for Voltages Measured by the High Speed Supervisor

VOUT_OV_FAULT_RESPONSE and VOUT_UV_FAULT_RESPONSE

The fault response documented here is for voltages that are measured by the high speed supervisor. These voltages are measured over a short period of time and may require a de-glitch period. Note that in addition to the response described by these commands, the LTC2978 will also:

- Set the appropriate bit(s) in the STATUS_BYTE
- Set the appropriate bit(s) in the STATUS_WORD
- Set the appropriate bit in the corresponding STATUS_VOUT register, and
- Notify the host by pulling the ALERTB pin low.

Note: Odd numbered channels configured for high resolution ADC measurements will not respond to OV/UV faults or warnings.

Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:6]	Vout_ov_fault_response_action, Vout_uv_fault_response_action	Response action. 2'b00: The unit continues operation without interruption. 2'b01: The unit continues operating for the delay time specified by bits[2:0] in increments of Ts_vs. If the fault is still present at the end of the delay time, the unit responds as programmed in the retry setting (bits [5:3]). 2'b1X: The device shuts down and responds according to the retry setting in bits [5:3].
b[5:3]	Vout_ov_fault_response_retry, Vout_uv_fault_response_retry	Response action: 3'b000: A zero value for the retry setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared. 3'b001-111: The PMBus device attempts to restart continuously, without limitation, using Mfr_retry_delay, until it is commanded OFF (by the CONTROL pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down.
b[2:0]	Vout_ov_fault_response_delay, Vout_uv_fault_response_delay	This sample count determines the amount of time a unit is to ignore a fault after it is first detected. Use this delay to de-glitch fast faults. 3'b000: The unit turns off immediately. 3'b001 – 3'b111: The unit turns off after b[2:0] samples at the sampling period of Ts_vs (12.2µs typical).

OPERATION

Fault Response for Values Measured by the ADC

OT_FAULT_RESPONSE, UT_FAULT_RESPONSE, VIN_OV_FAULT_RESPONSE and VIN_UV_FAULT_RESPONSE

The fault response documented here is for values that are measured by the ADC. These values are measured over a longer period of time and are not de-glitched. Note that in addition to the response described by these commands, the LTC2978 will also:

- Set the appropriate bit(s) in the STATUS_BYTE
- Set the appropriate bit(s) in the STATUS_WORD
- Set the appropriate bit in the corresponding STATUS_VIN or STATUS_TEMPERATURE register, and
- Notify the host by pulling the ALERTB pin low.

Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:6]	Ot_fault_response_action, Ut_fault_response_action, Vin_ov_fault_response_action, Vin_uv_fault_response_action	Response action: 2'b00: The unit continues operation without interruption. 2'b01: The device shuts down and responds according to the retry setting in bits [5:3]. 2'b10: The device shuts down and responds according to the retry setting in bits [5:3]. 2'b11: The device shuts down and responds according to the retry setting in bits [5:3].
b[5:3]	Ot_fault_response_retry, Ut_fault_response_retry, Vin_ov_fault_response_retry, Vin_uv_fault_response_retry	Response action: 3'b000: A zero value for the retry setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared. 3'b001-111: The PMBus device attempts to restart continuously, without limitation, using Mfr_retry_delay, until it is commanded OFF (by the CONTROL*n* pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down.
b[2:0]	Ot_fault_response_delay, Ut_fault_response_delay, Vin_ov_fault_response_delay, Vin_uv_fault_response_delay	Hard coded to 3'b000. The unit turns off immediately.

OPERATION

Timed Fault Response

TON_MAX_FAULT_RESPONSE

This command defines the LTC2978 response to a TON_MAX_FAULT. At start-up, the TON_MAX_FAULT_RESPONSE is disarmed once the output voltage reaches the VOUT_UNDER_VOLTAGE_LIMIT. The only way to protect against a short-circuited output at start-up is to take action in response to a TON_MAX_FAULT since VOUT_UV_FAULT_RESPONSE is not armed until the output reaches the VOUT_UNDER_VOLTAGE_LIMIT.

The device also:

- Sets the HIGH_BYTE bit in the STATUS_BYTE,
- Sets the VOUT bit in the STATUS_WORD,
- Sets the TON_MAX_FAULT bit in the STATUS_VOUT register, and
- Notifies the host by asserting ALERTB.

TON_MAX_FAULT_RESPONSE Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:6]	Ton_max_fault_response_action	Response action. 2'b00: The unit continues operation without interruption. 2'b01: The unit continues operating for the delay time specified which for this type of fault corresponds to an immediate shutdown. After shutting off, the device responds according to the retry settings in bits [5:3]. 2'b1X: The device shuts down and responds according to the retry setting in bits [5:3].
b[5:3]	Ton_max_fault_response_retry	Response action: 3'b000: A zero value for the Retry Setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared. 3'b001-111: The PMBus device attempts to restart continuously, without limitation, using Mfr_retry_delay, until it is commanded OFF (by the CONTROL*n* pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down.
b[2:0]	Ton_max_fault_response_delay	Hard coded to 3'b000. The unit turns off immediately.

OPERATION

STATUS_BYTE:

The STATUS_BYTE command returns the summary of the most critical faults or warnings which have occurred, as shown in the following table:

STATUS_BYTE Data Contents

BIT(S)	SYMBOL	OPERATION
b[7]	Status_byte_busy	Device busy when PMBus command received.
b[6]	Status_byte_off	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled.
b[5]	Status_byte_vout_ov	An output overvoltage fault has occurred.
b[4]	Status_byte_iout_oc	Not supported. Always returns 0.
b[3]	Status_byte_vin_uv	A V_{IN} undervoltage fault has occurred.
b[2]	Status_byte_temp	A temperature fault or warning has occurred.
b[1]	Status_byte_cml	A communication, memory or logic fault has occurred.
b[0]	Status_byte_high_byte	Fault/warning not listed in b[7:1].

STATUS_WORD:

The STATUS_WORD command returns two bytes of information with a summary of the unit's fault condition. Based on the information in these bytes, the host can get more information by reading the appropriate status byte.

The low byte of the STATUS_WORD is the same register as the STATUS_BYTE command.

STATUS_WORD Data Contents

BIT(S)	SYMBOL	OPERATION
b[15]	Status_word_vout	An output voltage fault or warning has occurred.
b[14]	Status_word_iout	Not supported. Always returns 0.
b[13]	Status_word_input	An input voltage fault or warning has occurred.
b[12]	Status_word_mfr	A manufacturer specific fault has occurred.
b[11]	Status_word_power_not_good	The POWER_GOOD signal, if present is negated. Power is not good.
b[10]	Status_word_cooling	Not supported. Always returns 0.
b[9]	Status_word_other	Not supported. Always returns 0.
b[8]	Status_word_unknown	Not supported. Always returns 0.
b[7]	Status_word_busy	Device busy when PMBus command received.
b[6]	Status_word_off	Status_byte_off
b[5]	Status_word_vout_ov	Status_byte_vout_ov
b[4]	Status_word_iout_oc	Not supported. Always returns 0.
b[3]	Status_word_vin_uv	Status_byte_vin_uv
b[2]	Status_word_temp	Status_byte_temp
b[1]	Status_word_cml	Status_byte_cml
b[0]	Status_word_high_byte	A bit in the high byte of the STATUS_WORD (b[15:8]) is set.

OPERATION

STATUS_VOUT

The STATUS_VOUT command returns the summary of the voltage faults or warnings which have occurred, as shown in the following table:

STATUS_VOUT Data Contents

BIT(S)	SYMBOL	OPERATION
b[7]	Status_vout_ov_fault	Overvoltage fault.
b[6]	Status_vout_ov_warn	Overvoltage warning.
b[5]	Status_vout_uv_warn	Undervoltage warning
b[4]	Status_vout_uv_fault	Undervoltage fault.
b[3]	Status_vout_max_fault	VOUT_MAX fault. An attempt has been made to set the output voltage to a value higher than allowed by the VOUT_MAX command.
b[2]	Status_vout_ton_max_fault	TON_MAX_FAULT sequencing fault.
b[1]	Status_vout_toff_max_warn	Not supported. Always returns 0.
b[0]	Status_vout_tracking_error	Not supported. Always returns 0.

STATUS_INPUT

The STATUS_INPUT command returns the summary of the V_{IN} faults or warnings which have occurred, as shown in the following table:

STATUS_INPUT Data Contents

BIT(S)	SYMBOL	OPERATION
b[7]	Status_input_ov_fault	V_{IN} Overvoltage fault
b[6]	Status_input_ov_warn	V_{IN} Overvoltage warning
b[5]	Status_input_uv_warn	V_{IN} Undervoltage warning
b[4]	Status_input_uv_fault	V_{IN} Undervoltage fault
b[3]	Status_input_off	Unit is off for insufficient input voltage.
b[2]	I_{IN} overcurrent fault	Not supported. Always returns 0.
b[1]	I_{IN} overcurrent warn	Not supported. Always returns 0.
b[0]	PIN overpower warn	Not supported. Always returns 0.

STATUS_TEMPERATURE

The STATUS_TEMPERATURE command returns the summary of the temperature faults or warnings which have occurred, as shown in the following table:

STATUS_TEMPERATURE Data Contents

Bit(s)	Symbol	Operation
b[7]	Status_temperature_ot_fault	Overtemperature fault.
b[6]	Status_temperature_ot_warn	Overtemperature warning.
b[5]	Status_temperature_ut_warn	Undertemperature warning.
b[4]	Status_temperature_ut_fault	Undertemperature fault.
b[3]	Reserved	Reserved. Always returns 0.
b[2]	Reserved	Reserved. Always returns 0.
b[1]	Reserved	Reserved. Always returns 0.
b[0]	Reserved	Reserved. Always returns 0.

STATUS_CML

The STATUS_CML command returns the summary of the communication, memory and logic faults or warnings which have occurred, as shown in the following table:

STATUS_CML Data Contents

BIT(S)	SYMBOL	OPERATION
b[7]	Status_cml_cmd_fault	1 = An illegal or unsupported command fault has occurred. 0 = No fault has occurred.
b[6]	Status_cml_data_fault	1 = Illegal or unsupported data received. 0 = No fault has occurred.
b[5]	Status_cml_pec_fault	1 = A PEC fault has occurred. 0 = No fault has occurred.
b[4]	Status_cml_memory_fault	1 = A fault has occurred in the NVM. 0 = No fault has occurred.
b[3]	Status_cml_processor_fault	Not supported, always returns 0.
b[2]	Reserved	Not supported, always returns 0.
b[1]	Status_cml_PMBus_fault	1 = A communication fault other than ones listed in this table has occurred. 0 = No fault has occurred.
b[0]	Status_cml_unknown_fault	Not supported, always returns 0.

OPERATION

STATUS_MFR_SPECIFIC

The STATUS_MFR_SPECIFIC command returns manufacturer specific status flags. Bits marked FAULT = No are intended to support polled handshaking; these are not latched nor do they assert ALERTB. Bits marked Channel = All can be read from any page. Bits marked FAULT = Yes assert ALERTB low and are cleared by CLEAR_FAULTS.

STATUS_MFR_SPECIFIC Data Contents

BIT(S)	SYMBOL	OPERATION	CHANNEL	FAULT
b[7]	Status_mfr_discharge	1 = A V_{OUT} discharge fault occurred while attempting to enter the ON state 0 = No V_{OUT} discharge fault has occurred	Current Page	Yes
b[6]	Status_mfr_fault1_in	This channel attempted to turn on while the FAULTBz1 pin was asserted low, or this channel has shut down at least once in response to a FAULTBz1 pin asserting low since the last CONTROL*n* pin toggle, OPERATION command ON/OFF cycle or CLEAR_FAULTS command.	Current Page	Yes
b[5]	Status_mfr_fault0_in	This channel attempted to turn on while the FAULTBz0 pin was asserted low, or this channel has shut down at least once in response to a FAULTBz0 pin asserting low since the last CONTROL*n* pin toggle, OPERATION command ON/OFF cycle or CLEAR_FAULTS command.	Current Page	Yes
b[4]	Status_mfr_servo_target_reached	Servo target has been reached.	Current Page	No
b[3]	Status_mfr_dac_connected	DAC is connected and driving V_{DACP} pin.	Current Page	No
b[2]	Status_mfr_dac_saturated	A previous servo operation terminated with maximum or minimum DAC value.	Current Page	Yes
b[1]	Status_mfr_vinen_faulted_off	V_{IN_EN} has been deasserted due to a VOUT fault.	All	No
b[0]	Status_mfr_watchdog_fault	1 = A watchdog fault has occurred. 0 = No watchdog fault has occurred.	All	Yes

OPERATION

ADC Monitoring Commands

READ_VIN

This command returns the most recent ADC measured value of the voltage measured at the V_{IN_SNS} pin.

READ_VIN Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:0]	Read_vin[15:0]	The data uses the linear format: $V(Symbol) = Y \cdot 2^N$ where N = b[15:11] is a 5-bit two's complement integer and Y = b[10:0] is an 11-bit two's complement integer Units: V

READ_VOUT

This command returns the most recent ADC measured value of the channel's output voltage. When odd channels are configured to measure current, the data contents have a slightly modified meaning, as described in the second table below.

READ_VOUT Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:0]	Read_vout[15:0]	The data uses the linear mode format as defined by VOUT_MODE: $V(Read\_vout) = Y \cdot 2^N$ where Y = b[15:0] is an unsigned integer and N = Vout_mode_ parameter is a 5-bit two's complement exponent that's hardwired to –13 decimal. Units: V.

READ_VOUT Data Contents—for Odd Channels Configured to Measure Current

Bit(s)	Symbol	Operation
b[15:0]	Read_vout[15:0]	The data uses the linear format: $V(Symbol) = Y \cdot 2^N$ where N = b[15:11] is a 5-bit two's complement integer and Y = b[10:0] is an 11-bit two's complement integer Units: mV

READ_TEMPERATURE_1

This command returns the most recent ADC measured value of junction temperature in °C as determined by the LTC2978's internal temperature sensor.

READ_TEMPERATURE_1 Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:0]	Read_temperature_1 [15:0]	The data uses the linear format: $Temp(Symbol) = Y \cdot 2^N$ Where N = b[15:11] is a 5-bit two's complement integer and Y = b[10:0] is an 11-bit two's complement integer Units: °C.

PMBUS_REVISION

The PMBUS_REVISION command register is read only and reports the LTC2978 compliance to the PMBus standard revision 1.1.

PMBUS_REVISION Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:0]	PMBus_rev	Reports the PMBus standard revision compliance. This is hard-coded to 'h11 for revision 1.1.

OPERATION

MANUFACTURER SPECIFIC COMMANDS

MFR_CONFIG:

This command is used to configure various manufacturer specific operating parameters for each channel.

MFR_CONFIG Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:12]	Reserved	Don't care. Always returns 0.
b[11]	Mfr_config_fast_servo_off	Disables fast servo when margining or trimming output voltages: 0: fast-servo enabled. 1: fast-servo disabled.
b[10]	Mfr_config_supervisor_resolution	Selects supervisor resolution: 0: high resolution – 4mV/LSB, range for V_{SENSEP} is 0V to 3.8V. 1: low resolution – 8mV/LSB, range for V_{SENSEP} is 0V to 6.0V.
b[9]	Mfr_config_adc_hires	Selects ADC resolution for odd channels. Ignored for even channels (they always use low res). 0: low resolution – 122µV/LSB. 1: high resolution – 15.6µV/LSB.
b[8]	Mfr_config_controln_sel	Selects the active control pin input (CONTROL0 or CONTROL1) for this channel. 0: Select CONTROL0 pin. 1: Select CONTROL1 pin.
b[7]	Mfr_config_servo_continuous	Select whether the UNIT should continuously servo V_{OUT} after it has reached a new margin or nominal target. Only applies when Mfr_dac_mode = 2'b00. 0: Do not continuously servo V_{OUT} after reaching initial target. 1: Continuously servo V_{OUT} to target.
b[6]	Mfr_config_servo_on_warn	Control re-servo on warning feature. Only applies when Mfr_config_dac_mode = 2'b00 and Mfr_config_servo_continuous = 0. 0: Do not allow the unit to re-servo when a V_{OUT} warning threshold is met or exceeded. 1: Allow the unit to re-servo V_{OUT} to nominal target if $V_{OUT} \geq$ V(Vout_ov_warn_limit) or $V_{OUT} \leq$ V(Vout_uv_warn_limit).
b[5:4]	Mfr_config_dac_mode	Determines how DAC is used when channel enters ON state or is already in ON state. 00: Soft connect (if needed) and servo to target. Wait for TON_RISE if just entering ON state. 01: DAC not connected. 10: DAC connected using value from MFR_DAC command. Does not wait for TON_RISE if just entering ON state. 11: DAC is soft connected. After soft connect is complete MFR_DAC may be written.
b[3]	Mfr_config_vo_en_wpu_en	V_{O_EN} charge pumped, current-limited pull-up enable. 0: Disable weak pull-up. V_{O_EN} driver is three-stated when channel is on. 1: Use weak current-limited pull-up on V_{O_EN} when the channel is on. For channels 4-7 this bit is treated as a 0 regardless of its value.
b[2]	Mfr_config_vo_en_wpd_en	V_{O_EN} current-limited pull-down enable. 0: Use a fast N-channel device to pull down V_{O_EN} when the channel is off for any reason. 1: Use weak current-limited pull-down to discharge V_{O_EN} when channel is off due to soft stop by the CONTROL*n* pin and/or OPERATION command. If the channel is off due to a fault, use the fast pull-down on V_{O_EN}. For channels 4-7 this bit is treated as a 0 regardless of its value.
b[1]	Mfr_config_dac_gain	DAC buffer gain. 0: Select DAC buffer gain dac_gain_0 (1.38V full-scale) 1: Select DAC buffer gain dac_gain_1 (2.65V full-scale)
b[0]	Mfr_config_dac_pol	DAC output polarity. 0: Encodes negative (inverting) DC/DC converter trim input. 1: Encodes positive (noninverting) DC/DC converter trim input.

OPERATION

MFR_CONFIG_ALL:

This command is used to configure parameters that are common to all channels on the IC. They may be set or reviewed from any PAGE setting.

MFR_CONFIG_ALL Data Contents

BIT(S)	SYMBOL	OPERATION
b[7]	Mfr_config_fault_log_enable	Enable fault logging to NVM in response to Fault. 0: Fault logging to NVM is disabled 1: Fault logging to NVM is enabled
b[6]	Mfr_vin_on_clr_faults_en	VIN_ON rising edge to clear all latched faults 0: VIN_ON clear faults feature is disabled 1: VIN_ON clear faults feature is enabled
b[5]	Mfr_config_control1_pol	Selects active polarity of control1 pin. 0: Active low (pull pin low to start unit) 1: Active high (pull pin high to start unit)
b[4]	Mfr_config_control0_pol	Selects active polarity of control0 pin. 0: Active low (pull pin low to start unit) 1: Active high (pull pin high to start unit)

MFR_CONFIG_ALL Data Contents

b[3]	Mfr_config_vin_share_enable	Allow this unit to hold share-clock pin low when VIN_ON has fallen below VIN_OFF. When enabled, this unit will also turn all channels off in response to share-clock being held low. 0: Share-clock inhibit is disabled 1: Share-clock inhibit is enabled
b[2]	Mfr_config_all_pec_en	PMBus packet error checking enable. 0: PEC is accepted but not required 1: PEC is required
b[1]	Mfr_config_all_longer_pmbus_timeout	Increase PMBus timeout internal by a factor of 8. 0: PMBus timeout is not multiplied by a factor of 8 1: PMBus timeout is multiplied by a factor of 8
b[0]	Mfr_config_all_vinen_wpu_dis	V_{IN_EN} charge pumped, current-limited pull-up disable. 0: Use weak current-limited pull-up on V_{IN_EN} after power-up, as long as no faults have forced V_{IN_EN} off. 1: Disable weak pull-up. V_{IN_EN} driver is three-stated after power-up as long as no faults have forced V_{IN_EN} off.

OPERATION

MFR_FAULTB00_PROPAGATE, MFR_FAULTB01_PROPAGATE, MFR_FAULTB10_PROPAGATE and MFR_FAULTB11_PROPAGATE

These manufacturer specific commands enable channels that have faulted off to propagate that state to the appropriate fault pin. There are two zones in the LTC2978. In zone 0, faulted off states for channels 0 through 3 can be propagated to FAULT00 or FAULT01. In zone 1, faulted off states for channels 4 through 7 can be propagated to FAULT10 or FAULT11. See Figure 13.

MFR_FAULTB00_PROPAGATE Data Contents—Fault Zone 0 (Pages 0-3)

BIT(S)	SYMBOL	OPERATION
b[7:1]	Reserved	Don't care. Always returns 0.
b[0]	Mfr_faultb00_propagate	Enable fault propagation. 0: FAULTB00 will not be affected if a fault is declared. 1: FAULTB00 will be asserted low if a fault is declared.

MFR_FAULTB01_PROPAGATE Data Contents—Fault Zone 0 (Pages 0-3)

BIT(S)	SYMBOL	OPERATION
b[7:1]	Reserved	Don't care. Always returns 0.
b[0]	Mfr_faultb01_propagate	Enable fault propagation. 0: FAULTB01 will not be affected if a fault is declared. 1: FAULTB01 will be asserted low if a fault is declared.

MFR_FAULTB10_PROPAGATE Data Contents—Fault Zone 1 (Pages 4-7)

BIT(S)	SYMBOL	OPERATION
b[7:1]	Reserved	Don't care. Always returns 0.
b[0]	Mfr_faultb10_propagate	Enable fault propagation. 0: FAULTB10 will not be affected if a fault is declared. 1: FAULTB10 will be asserted low if a fault is declared.

MFR_FAULTB11_PROPAGATE Data Contents—Fault Zone 1 (Pages 4-7)

BIT(S)	SYMBOL	OPERATION
b[7:1]	Reserved	Don't care. Always returns 0.
b[0]	Mfr_faultb11_propagate	Enable fault propagation. 0: FAULTB11 will not be affected if a fault is declared. 1: FAULTB11 will be asserted low if a fault is declared.

OPERATION

MFR_PWRGD_EN

This command register controls the mapping of power good status to the power good pin. Note that odd numbered channels whose ADC is in high res mode do not contribute to power good.

MFR_PWRGD_EN Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:9]	Reserved	Read only, always returns 0s.
b[8]	Mfr_pwrgd_en_wdog	Watchdog 1 = Watchdog timer not-expired status is ANDed with PWRGD status for any similarly enabled channels to determine when the PWRGD pin gets asserted. 0 = Watchdog timer does not affect the PWRGD pin.
b[7]	Mfr_pwrgd_en_chan7	Channel 7 1 = PWRGD status for this channel is ANDed with PWRGD status for any similarly enabled channels to determine when the PWRGD pin gets asserted. 0 = PRWGD status for this channel does not affect the PWRGD pin.
b[6]	Mfr_pwrgd_en_chan6	Channel 6 1 = PWRGD status for this channel is ANDed with PWRGD status for any similarly enabled channels to determine when the PWRGD pin gets asserted. 0 = PRWGD status for this channel does not affect the PWRGD pin.
b[5]	Mfr_pwrgd_en_chan5	Channel 5 1 = PWRGD status for this channel is ANDed with PWRGD status for any similarly enabled channels to determine when the PWRGD pin gets asserted. 0 = PRWGD status for this channel does not affect the PWRGD pin.
b[4]	Mfr_pwrgd_en_chan4	Channel 4 1 = PWRGD status for this channel is ANDed with PWRGD status for any similarly enabled channels to determine when the PWRGD pin gets asserted. 0 = PRWGD status for this channel does not affect the PWRGD pin.
b[3]	Mfr_pwrgd_en_chan3	Channel 3 1 = PWRGD status for this channel is ANDed with PWRGD status for any similarly enabled channels to determine when the PWRGD pin gets asserted. 0 = PRWGD status for this channel does not affect the PWRGD pin.
b[2]	Mfr_pwrgd_en_chan2	Channel 2 1 = PWRGD status for this channel is ANDed with PWRGD status for any similarly enabled channels to determine when the PWRGD pin gets asserted. 0 = PRWGD status for this channel does not affect the PWRGD pin.
b[1]	Mfr_pwrgd_en_chan1	Channel 1 1 = PWRGD status for this channel is ANDed with PWRGD status for any similarly enabled channels to determine when the PWRGD pin gets asserted. 0 = PRWGD status for this channel does not affect the PWRGD pin.
b[0]	Mfr_pwrgd_en_chan0	Channel 0 1 = PWRGD status for this channel is ANDed with PWRGD status for any similarly enabled channels to determine when the PWRGD pin gets asserted. 0 = PRWGD status for this channel does not affect the PWRGD pin.

OPERATION

MFR_FAULTB00_RESPONSE, MFR_FAULTB01_RESPONSE, MFR_FAULTB10_RESPONSE and MFR_FAULTB11_RESPONSE

These manufacturer specific commands share the same format and specify the response to assertions of the bidirectional fault pins. For fault zone 0, MFR_FAULTB00_RESPONSE determines how channels 0-3 respond when the FAULTB00 pin is asserted, and MFR_FAULTB01_RESPONSE determines how channels 0-3 respond when the FAULTB01 pin is asserted. For fault zone 1, MFR_FAULTB10_RESPONSE determines how channels 4-7 respond when the FAULTB10 pin is asserted, and MFR_FAULTB11_RESPONSE determines how channels 4-7 respond when the FAULTB11 pin is asserted. If one or more bits in the MFR_FAULTBz*n*_RESPONSE registers are set, a FAULTBz*n* assertion will cause the ALERTB pin to assert low and set the appropriate bit in the STATUS_MFR_SPECIFIC register.

Data Contents—Fault Zone 0 Response Commands

BIT(S)	SYMBOL	OPERATION
b[7:4]	Reserved	Read only, always returns 0s.
b[3]	Mfr_faultb00_response_chan3, Mfr_faultb01_response_chan3	Channel 3 response. 0: The channel continues operation without interruption. 1: The channel shuts down if the corresponding FAULTBz*n* pin is still asserted after 10µs. When the FAULTBz*n* pin subsequently deasserts, the channel turns back on, honoring TON_DELAY and TON_RISE settings.
b[2]	Mfr_faultb00_response_chan2, Mfr_faultb01_response_chan2	Channel 2 response. 0: The channel continues operation without interruption. 1: The channel shuts down if the corresponding FAULTBz*n* pin is still asserted after 10µs. When the FAULTBz*n* pin subsequently deasserts, the channel turns back on, honoring TON_DELAY and TON_RISE settings.
b[1]	Mfr_faultb00_response_chan1, Mfr_faultb01_response_chan1	Channel 1 response. 0: The channel continues operation without interruption. 1: The channel shuts down if the corresponding FAULTBz*n* pin is still asserted after 10µs. When the FAULTBz*n* pin subsequently deasserts, the channel turns back on, honoring TON_DELAY and TON_RISE settings.
b[0]	Mfr_faultb00_response_chan0, Mfr_faultb01_response_chan0	Channel 0 response. 0: The channel continues operation without interruption. 1: The channel shuts down if the corresponding FAULTBz*n* pin is still asserted after 10µs. When the FAULTBz*n* pin subsequently deasserts, the channel turns back on, honoring TON_DELAY and TON_RISE settings.

Data Contents—Fault Zone 1 Response Commands

BIT(S)	SYMBOL	OPERATION
b[7:4]	Reserved	Read only, always returns 0s.
b[3]	Mfr_faultb10_response_chan7, Mfr_faultb11_response_chan7	Channel 7 response. 0: The channel continues operation without interruption. 1: The channel shuts down if the corresponding FAULTBz*n* pin is still asserted after 10µs. When the FAULTBz*n* pin subsequently deasserts, the channel turns back on, honoring TON_DELAY and TON_RISE settings.
b[2]	Mfr_faultb10_response_chan6, Mfr_faultb11_response_chan6	Channel 6 response. 0: The channel continues operation without interruption. 1: The channel shuts down if the corresponding FAULTBz*n* pin is still asserted after 10µs. When the FAULTBz*n* pin subsequently deasserts, the channel turns back on, honoring TON_DELAY and TON_RISE settings.
b[1]	Mfr_faultb10_response_chan5, Mfr_faultb11_response_chan5	Channel 5 response. 0: The channel continues operation without interruption. 1: The channel shuts down if the corresponding FAULTBz*n* pin is still asserted after 10µs. When the FAULTBz*n* pin subsequently deasserts, the channel turns back on, honoring TON_DELAY and TON_RISE settings.
b[0]	Mfr_faultb10_response_chan4, Mfr_faultb11_response_chan4	Channel 4 response. 0: The channel continues operation without interruption. 1: The channel shuts down if the corresponding FAULTBz*n* pin is still asserted after 10µs. When the FAULTBz*n* pin subsequently deasserts, the channel turns back on, honoring TON_DELAY and TON_RISE settings.

OPERATION

MFR_VINEN_OV_FAULT_RESPONSE

This command register determines whether V_{OUT} over voltage faults from a given channel cause the V_{IN_EN} pin to be forced off.

MFR_VINEN_OV_FAULT_RESPONSE Data Contents

BIT(S)	SYMBOL	OPERATION
b[7]	Mfr_vinen_ov_fault_response_chan7	Response to channel 7 VOUT_OV_FAULT. 1 = Disable V_{IN_EN} via fast pull-down. 0 = Leave V_{IN_EN} as-is.
b[6]	Mfr_vinen_ov_fault_response_chan6	Response to channel 6 VOUT_OV_FAULT. 1 = Disable V_{IN_EN} via fast pull-down. 0 = Leave V_{IN_EN} as-is.
b[5]	Mfr_vinen_ov_fault_response_chan5	Response to channel 5 VOUT_OV_FAULT. 1 = Disable V_{IN_EN} via fast pull-down. 0 = Leave V_{IN_EN} as-is.
b[4]	Mfr_vinen_ov_fault_response_chan4	Response to channel 4 VOUT_OV_FAULT. 1 = Disable V_{IN_EN} via fast pull-down. 0 = Leave V_{IN_EN} as-is.
b[3]	Mfr_vinen_ov_fault_response_chan3	Response to channel 3 VOUT_OV_FAULT. 1 = Disable V_{IN_EN} via fast pull-down. 0 = Leave V_{IN_EN} as-is.
b[2]	Mfr_vinen_ov_fault_response_chan2	Response to channel 2 VOUT_OV_FAULT. 1 = Disable V_{IN_EN} via fast pull-down. 0 = Leave V_{IN_EN} as-is.
b[1]	Mfr_vinen_ov_fault_response_chan1	Response to channel 1 VOUT_OV_FAULT. 1 = Disable V_{IN_EN} via fast pull-down. 0 = Leave V_{IN_EN} as-is.
b[0]	Mfr_vinen_ov_fault_response_chan0	Response to channel 0 VOUT_OV_FAULT. 1 = Disable V_{IN_EN} via fast pull-down. 0 = Leave V_{IN_EN} as-is.

OPERATION

MFR_VINEN_UV_FAULT_RESPONSE

This command register determines whether V_{OUT} under voltage faults from a given channel cause the V_{IN_EN} pin to be forced off.

MFR_VINEN_UV_FAULT_RESPONSE Data Contents

BIT(S)	SYMBOL	OPERATION
b[7]	Mfr_vinen_uv_fault_response_chan7	Response to channel 7 VOUT_UV_FAULT. 1 = Disable V_{IN_EN} via fast pull-down. 0 = Leave V_{IN_EN} as-is.
b[6]	Mfr_vinen_uv_fault_response_chan6	Response to channel 6 VOUT_UV_FAULT. 1 = Disable V_{IN_EN} via fast pull-down. 0 = Leave V_{IN_EN} as-is.
b[5]	Mfr_vinen_uv_fault_response_chan5	Response to channel 5 VOUT_UV_FAULT. 1 = Disable V_{IN_EN} via fast pull-down. 0 = Leave V_{IN_EN} as-is.
b[4]	Mfr_vinen_uv_fault_response_chan4	Response to channel 4 VOUT_UV_FAULT. 1 = Disable V_{IN_EN} via fast pull-down. 0 = Leave V_{IN_EN} as-is.
b[3]	Mfr_vinen_uv_fault_response_chan3	Response to channel 3 VOUT_UV_FAULT. 1 = Disable V_{IN_EN} via fast pull-down. 0 = Leave V_{IN_EN} as-is.
b[2]	Mfr_vinen_uv_fault_response_chan2	Response to channel 2 VOUT_UV_FAULT. 1 = Disable V_{IN_EN} via fast pull-down. 0 = Leave V_{IN_EN} as-is.
b[1]	Mfr_vinen_uv_fault_response_chan1	Response to channel 1 VOUT_UV_FAULT. 1 = Disable V_{IN_EN} via fast pull-down. 0 = Leave V_{IN_EN} as-is.
b[0]	Mfr_vinen_uv_fault_response_chan0	Response to channel 0 VOUT_UV_FAULT. 1 = Disable V_{IN_EN} via fast pull-down. 0 = Leave V_{IN_EN} as-is.

OPERATION

MFR_RETRY_DELAY

This command determines the retry interval when the LTC2978 is in hiccup mode in response to a fault condition.

MFR_RETRY_DELAY Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:0]	Mfr_retry_delay	The data uses the linear format: $T(Symbol) = Y \cdot 2^N$ Where N = b[15:11] is a 5-bit two's complement integer and Y = b[10:0] is an 11-bit two's complement integer This delay is counted using SHARE_CLK only. Delays are rounded to the nearest 200µs. Units: ms. Max delay is 13.1 sec.

MFR_RESTART_DELAY

This command determines how the CONTROL*n* pins are adjusted before use. The time the adjusted version of the CONTROL*n* pin is in the off polarity is stretched by this command to be at least Mfr_restart_delay ms. CONTROL*n* pin transitions whose OFF time exceeds Mfr_restart_delay are not affected by this command. A value of all zeros disables this feature.

MFR_RESTART_DELAY Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:0]	Mfr_restart_delay	The data uses the linear format: $T(Symbol) = Y \cdot 2^N$ Where N = b[15:11] is a 5-bit two's complement integer and Y = b[10:0] is an 11-bit two's complement integer This delay is counted using SHARE_CLK only. Delays are rounded to the nearest 200µs. Units: ms. Max delay is 13.1 sec.

MFR_VOUT_PEAK

This command returns the maximum ADC measured value of the channel's output voltage. This command is not supported for odd channels that are configured to measure current. This register is reset to zero when the LTC2978 emerges from power-on reset or when a CLEAR_FAULTS command is executed.

MFR_VOUT_PEAK Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:0]	Mfr_vout_peak[15:0]	The data uses the linear mode format as defined by VOUT_MODE: $V(mfr\_vout\_peak) = Y \cdot 2^N$ where Y = b[15:0] is an unsigned integer and N = Vout_mode_parameter is a 5-bit two's complement exponent that's hardwired to –13 decimal. Units: V.

MFR_VIN_PEAK

This command returns the maximum ADC measured value of the input voltage. The contents of this register are reset to 'h7C00 when the LTC2978 emerges from power-on reset or when a CLEAR_FAULTS command is executed.

MFR_VIN_PEAK Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:0]	Mfr_vin_peak[15:0]	The data uses the linear format: $V(Symbol) = Y \cdot 2^N$ where N = b[15:11] is a 5-bit two's complement integer and Y = b[10:0] is an 11-bit two's complement integer Units: V

MFR_TEMPERATURE_PEAK

This command returns the maximum ADC measured value of junction temperature in °C as determined by the LTC2978's internal temperature sensor. The contents

OPERATION

of this register are reset to 'h7C00 when the LTC2978 emerges from power-on reset or when a CLEAR_FAULTS command is executed.

MFR_TEMPERATURE_PEAK Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:0]	Mfr_temperature_peak[15:0]	The data uses the linear format: $V(Symbol) = Y \cdot 2^N$ Where N = b[15:11] is a 5-bit two's complement integer and Y = b[10:0] is an 11-bit two's complement integer Units: °C.

MFR_DAC

This command register returns the 10-bit value for the voltage-buffered current DAC. This register may be written when Mfr_config_dac_mode is configured for either of the two manual DAC modes.

MFR_DAC Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:10]	Reserved	Read only, always returns 'h3F.
b[9:0]	Mfr_dac_direct_val	Voltage-buffered current DAC code value.

MFR_POWERGOOD_ASSERTION_DELAY

This command register allows the user to program the delay from when the internal power good signal becomes valid until the power good output is asserted.

MFR_POWERGOOD_ASSERTION_DELAY Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:0]	Mfr_powergood_assertion_delay	The data uses the linear format: $T(Symbol) = Y \cdot 2^N$ Where N = b[15:11] is a 5-bit two's complement integer and Y = b[10:0] is an 11-bit two's complement integer. This delay is counted using internal clock independent of SHARE_CLK. Delays are rounded to the nearest 200µs Units: ms. Max delay is 13.1 sec.

MFR_WATCHDOG_T_FIRST and MFR_WATCHDOG_T

The MFR_WATCHDOG_T_FIRST register allows the user to program the duration of the first watchdog timer interval following assertion of the POWER GOOD signal, assuming the POWER GOOD signal reflects the status of the watchdog timer. If assertion of POWER GOOD is not conditioned by the watchdog timer's status, then MFR_WATCHDOG_T_FIRST applies to the first timing interval after the timer is enabled. Writing a value of 0ms to the MFR_WATCHDOG_T_FIRST register disables the watchdog timer.

The MFR_WATCHDOG_T register allows the user to program watchdog time intervals subsequent to the MFR_WATCHDOG_T_FIRST timing interval. Writing a value of 0ms to the MFR_WATCHDOG_T register disables the watchdog timer. A non-zero write to MFR_WATCHDOG_T will reset the watchdog timer.

MFR_WATCHDOG_T_POR and MFR_WATCHDOG_T Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:0]	Mfr_watchdog_t_first Mfr_watchdog_t	The data uses the linear format: $T(Symbol) = Y \cdot 2^N$ Where N = b[15:11] is a 5-bit two's complement integer and Y = b[10:0] is an 11-bit two's complement integer These timers operate on an internal clock independent of SHARE_CLK. Delays are rounded to the nearest 10µs for _t and 1ms for _t_first. Writing a zero value for Y to the Mfr_watchdog_t or Mfr_watchdog_t_first registers will disable the watchdog timer. Units: ms. Max timeout is 0.6 sec for _t and 65 sec for _t_first

OPERATION

MFR_PAGE_FF_MASK

The MFR_PAGE_FF_MASK command is used to select which channels respond when the global page (FF) is in use. Note that the only commands that support PAGE = 'hFF are OPERATION and ON_OFF_CONFIG.

MFR_PAGE_FF_MASK Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:0]	Mfr_page_ff_mask	Global page response enable, per channel Each bit enables/disables the corresponding channel: 0 = ignore global page accesses 1 = fully respond to global page accesses

MFR_PADS

The MFR_PADS command provides read only access to slow frequency digital pads. The input values presented in bits[9:0] are before any deglitching logic.

MFR_PADS_PWRGD_DRIVE Data Contents

BIT(S)	SYMBOL	OPERATION
b[15]	Mfr_pads_pwrgd_drive	0 = PWRGD pad is being driven low by this chip 1 = PWRGD pad is not being driven low by this chip
b[14]	Mfr_pads_alertb_drive	0 = ALERTB pad is being driven low by this chip 1 = ALERTB pad is not being driven low by this chip
b[13:10]	Mfr_pads_faultb_drive[3.0]	Bit[3] used for FAULTB00 pad, bit[2] used for FAULTB01 pad, bit[1] used for FAULTB10 pad, bit[0] used for FAULTB11 pad as follows: 0 = FAULTB pad is being driven low by this chip 1 = FAULTB pad is not being driven low by this chip
b[9:8]	Mfr_pads_asel1[1:0]	11: Logic high detected on ASEL1 input pad 10: ASEL1 input pad is floating 01: Reserved 00: Logic low detected on ASEL1 input pad
b[7:6]	Mfr_pads_asel0[1:0]	11: Logic high detected on ASEL0 input pad 10: ASEL0 input pad is floating 01: Reserved 00: Logic low detected on ASEL0 input pad
b[5]	Mfr_pads_control1	1: Logic high detected on CONTROL1 pad 0: Logic low detected on CONTROL1 pad
b[4]	Mfr_pads_control0	1: Logic high detected on CONTROL0 pad 0: Logic low detected on CONTROL0 pad
b[3:0]	Mfr_pads_faultb[3:0]	Bit[3] used for FAULTB00 pad, bit[2] used for FAULTB01 pad, bit[1] used for FAULTB10 pad, bit[0] used for FAULTB11 pad as follows: 1: Logic high detected on FAULTBz*n* pad 0: Logic low detected on FAULTBz*n* pad

MFR_I2C_BASE_ADDRESS

The MFR_I2C_BASE_ADDRESS command determines the base value for the I^2C address byte.

MFR_I2C_BASE_ADDRESS Data Contents

BIT(S)	SYMBOL	OPERATION
b[7]	Reserved	Read only, always returns 0.
b[6:0]	i2c_base_address	This 7-bit value determines the base value of the 7-bit I^2C address.

MFR_SPECIAL_ID

This register contains the manufacturer ID for the LTC2978.

MFR_SPECIAL_ID Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:0]	Mfr_special_id	Read only, always returns 'h0121

MFR_SPECIAL_LOT

These paged registers contain information that identifies the user configuration that was programmed at the factory.

MFR_SPECIAL_LOT Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:0]	Mfr_special_lot	Contains the LTC default special lot number. Contact the factory to request a custom factory programmed user configuration and special lot number.

OPERATION

MFR_VOUT_DISCHARGE_THRESHOLD

This register contains the coefficient that multiplies VOUT_COMMAND in order to determine the OFF threshold voltage for the associated output. If the output voltage has not decayed below MFR_VOUT_DISCHARGE_THRESHOLD • VOUT_COMMAND prior to the channel being commanded to enter/re-enter the ON state, bit [7] in the STATUS_MFR_SPECIFIC register will be set and the ALERTB pin will be asserted low. In addition, the channel will not enter the ON state until the output has decayed below its OFF threshold voltage.

Other channels can be held off if a particular output has failed to discharge by using the bidirectional FAULTz*n* pins (refer to the MFR_FAULTBz*n*_RESPONSE and MFR_FAULTBz*n*_PROPAGATE registers).

MFR_VOUT_DISCHARGE_THRESHOLD Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:0]	Mfr_vout_discharge_threshold	The data uses the linear format: $k = Y \cdot 2^N$ Where N=b[15:11] is a 5-bit two's complement integer and Y= b[10:0] is an 11-bit two's complement integer. Units: Dimensionless, this register contains a coefficient.

MFR_FAULT_LOG_STORE

This command allows the user to transfer data from the RAM buffer to EEPROM.

MFR_FAULT_LOG_RESTORE

This command allows the user to transfer a copy of the fault-log data from the EEPROM to the RAM buffer. After a restore the RAM buffer is locked until a successful Mfr_fault_log read.

MFR_FAULT_LOG_CLEAR

This command initializes the EEPROM block reserved for fault logging. Any previous fault log stored in EEPROM will be erased by this operation.

MFR_FAULT_LOG_STATUS

Read only. This register is used to manage fault log events.

Mfr_fault_log_status_eeprom is set after a MFR_FAULT_LOG_STORE command or a faulted-off event triggers a transfer of the fault log from RAM to EEPROM. This bit is cleared by a MFR_FAULT_LOG_CLEAR command.

Mfr_fault_log_status_ram is set after a MFR_FAULT_LOG_RESTORE to indicate that the data in the RAM has been restored from EEPROM and not yet read using a MFR_FAULT_LOG command. This bit is cleared by a MFR_FAULT_LOG command.

MFR_FAULT_LOG_STATUS Data Contents

BIT(S)	SYMBOL	OPERATION
b[1]	Mfr_fault_log_status_ram	Fault log RAM status: 0: The fault log RAM allows updates. 1: The fault log RAM is locked until the next Mfr_fault_log read.
b[0]	Mfr_fault_log_status_eeprom	Fault log EEPROM status: 0: The transfer of the fault log RAM to the EEPROM is enabled. 1: The transfer of the fault log RAM to the EEPROM is inhibited.

OPERATION

MFR_FAULT_LOG

Read only. This 2048-bit data block contains a copy of the RAM buffer fault log. The RAM buffer is continuously updated after each ADC conversion as long as Mfr_fault_log_status_ram is clear. With Mfr_config_fault_log_en = 1 and Mfr_fault_log_status_eeprom = 0, the RAM buffer is transferred to EEPROM whenever an LTC2978 fault causes a channel to latch off or a MFR_FAULT_LOG_STORE command is received. Mfr_fault_log_status_eeprom is set high after the RAM buffer is transferred to EEPROM and not cleared until a Mfr_fault_log_clear is received; even if the LTC2978 is reset or powered down. Fault log EEPROM transfers are not initiated as a result of Status_mfr_discharge, Status_mfr_fault1_in or Status_mfr_fault0_in events. During a Mfr_fault_log read, data is returned one byte at a time as defined by the following table. The fault log stores approximately 1 to 2 seconds of telemetry.

MFR_FAULT_LOG Data Block Contents

DATA	BYTE	BLOCK READ COMMAND
Position_last[7:0]	0	Position of fault log pointer when fault occurred.
SharedTime[7:0]	1	41-bit share-clock counter value when fault occurred. Counter LSB is in 200µs increments. This counter is cleared at power-up or after the LTC2978 is reset
SharedTime[15:8]	2	
SharedTime[23:16]	3	
SharedTime[31:24]	4	
SharedTime[39:32]	5	
SharedTime[40]	6	
Mfr_vout_peak0[7:0]	7	
Mfr_vout_peak0[15:8]	8	
Mfr_vout_min0[7:0]	9	
Mfr_vout_min0[15:8]	10	
Mfr_vout_peak1[7:0]	11	
Mfr_vout_peak1[15:8]	12	
Mfr_vout_min1[7:0]	13	
Mfr_vout_min1[15:8]	14	
Mfr_vin_peak[7:0]	15	
Mfr_vin_peak[15:8]	16	
Mfr_vin_min[7:0]	17	

MFR_FAULT_LOG Data Block Contents

DATA	BYTE	BLOCK READ COMMAND
Mfr_vin_min[15:8]	18	
Mfr_vout_peak2[7:0]	19	
Mfr_vout_peak2[15:8]	20	
Mfr_vout_min2[7:0]	21	
Mfr_vout_min2[15:8]	22	
Mfr_vout_peak3[7:0]	23	
Mfr_vout_peak3[15:8]	24	
Mfr_vout_min3[7:0]	25	
Mfr_vout_min3[15:8]	26	
Mfr_temp_peak[7:0]	27	
Mfr_temp_peak[15:8]	28	
Mfr_ temp_min[7:0]	29	
Mfr_ temp_min[15:8]	30	
Mfr_vout_peak4[7:0]	31	
Mfr_vout_peak4[15:8]	32	
Mfr_vout_min4[7:0]	33	
Mfr_vout_min4[15:8]	34	
Mfr_vout_peak5[7:0]	35	
Mfr_vout_peak5[15:8]	36	
Mfr_vout_min5[7:0]	37	
Mfr_vout_min5[15:8]	38	
Mfr_vout_peak6[7:0]	39	
Mfr_vout_peak6[15:8]	40	
Mfr_vout_min6[7:0]	41	
Mfr_vout_min6[15:8]	42	
Mfr_vout_peak7[7:0]	43	
Mfr_vout_peak7[15:8]	44	
Mfr_vout_min7[7:0]	45	
Mfr_vout_min7[15:8]	46	
		47 bytes for preamble
Fault_log [Position_last]	47	
Fault_log [Position_last-1]	48	
.		
.		
.		
Fault_log [Position_last-201]	247	
Reserved	248-255	
		Number of loops (248-47)/40 = 5

OPERATION

Data is logged into memory in the order shown in the following table.

When data is returned during a block read it is returned in reverse order based on the value of Position_last[7:0]. Data byte Read_vout0[7:0] is followed by Status_mfr of page 7. Example: If Position_last = 9 then the first data returned in byte position 47 of a block read is Read_vin[15:8] followed by Read_vin[7:0] followed by Status_mfr of page 1.

POSITION	DATA
0	Read_vout0[7:0]
1	Read_vout0[15:8]
2	Status_vout0
3	Status_mfr0
4	Read_vout1[7:0]
5	Read_vout1[15:8]
6	Status_vout1
7	Status_mfr1
8	Read_vin[7:0]
9	Read_vin[15:8]
10	Status_vin
11	Reserved
12	Read_vout2[7:0]
13	Read_vout2[15:8]
14	Status_vout2
15	Status_mfr2
16	Read_vout3[7:0]
17	Read_vout3[15:8]
18	Status_vout3
19	Status_mfr3
20	Read_temperature_1[7:0]
21	Read_temperature_1[15:8]
22	Status_temp
23	Reserved
24	Read_vout4[7:0]
25	Read_vout4[15:8]
26	Status_vout4
27	Status_mfr4
28	Read_vout5[7:0]
29	Read_vout5[15:8]
30	Status_vout5
31	Status_mfr5
32	Read_vout6[7:0]
33	Read_vout6[15:8]
34	Status_vout6
35	Status_mfr6
36	Read_vout7[7:0]
37	Read_vout7[15:8]
38	Status_vout7
39	Status_mfr7
	Total Bytes =40

MFR_COMMON

This command returns status information for the share-clock pin (SCLK) and the write-protect pin (WP).

MFR_COMMON Data Contents

BIT(S)	SYMBOL	OPERATION
b[7:2]	Reserved	Read only, always returns 0s
b[1]	Mfr_common_share_clk	Returns status of share-clock pin 1: Share-clock pin is being held low 0: Share-clock pin is active
b[0]	Mfr_common_write_protect	Returns status of write-protect pin 1: Write-protect pin is high 0: Write-protect pin is low

MFR_SPARE0

This 16-bit wide registers can be used to store miscellaneous information. The contents of these registers may be stored and recalled from EEPROM using the STORE_USER_ALL and RESTORE_USER_ALL commands, respectively.

MFR_SPARE2

These 16-bit wide, paged registers can be used to store miscellaneous information. The contents of these registers may be stored and recalled from EEPROM using the STORE_USER_ALL and RESTORE_USER_ALL commands, respectively.

OPERATION

MFR_VOUT_MIN

This command returns the minimum ADC measured value of the channel's output voltage. The contents of this register is reset to 'hFFFF when the LTC2978 emerges from power-on reset or when a CLEAR_FAULTS command is executed. When odd channels are configured to measure current, this command is not supported.

MFR_VOUT_MIN Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:0]	Mfr_vout_min	The data uses the linear mode format as defined by VOUT_MODE: $V(mfr\_vout\_min) = Y \cdot 2^N$ Where Y = b[15:0] is an unsigned integer and N = Vout_mode_parameter is a 5-bit two's complement exponent that's hardwired to a value of –13 decimal. Units: V.

MFR_VIN_MIN

This command returns the minimum ADC measured value of the input voltage. The contents of this register is reset to 'h7BFF when the LTC2978 emerges from power-on reset or when a CLEAR_FAULTS command is executed. Updates are disabled when unit is off for insufficient input voltage.

MFR_VIN_MIN Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:0]	Mfr_vin_min	The data uses the linear format: $V(mfr\_vin\_min) = Y \cdot 2^N$ Where N = b[15:11] is a 5-bit two's complement integer and Y = b[10:0] is an 11-bit two's complement integer Units: V.

MFR_TEMPERATURE_MIN

This command returns the minimum ADC measured value of junction temperature in °C as determined by the LTC2978's internal temperature sensor. The contents of this register is reset to 'h7BFF when the LTC2978 emerges from power-on reset or when a CLEAR_FAULTS command is executed.

MFR_TEMPERATURE_MIN Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:0]	Mfr_temperature_min	The data uses the linear format: $V(mfr\_vin\_min) = Y \cdot 2^N$ Where N = b[15:11] is a 5-bit two's complement integer and Y = b[10:0] is an 11-bit two's complement integer Units: °C.

OPERATION

WATCHDOG

A non-zero write to the MFR_WATCHDOG_T register will reset the watchdog timer. Low-to-high transitions on the WDI pin also reset the watchdog timer. If the timer expires, ALERTB is asserted and the PWRGD output is optionally deasserted and then reasserted after MFR_PWRGD_ASSERTION_DELAY ms. Writing 0 to either the MFR_WATCHDOG_T or MFR_WATCHDOG_T_FIRST registers will disable the timer.

RESET

Holding the WDI pin low for more than t_{RESETB} will cause the LTC2978 to enter the power-on reset state. Following the subsequent rising-edge of the WDI pin, the LTC2978 will execute its power-on sequence per the user configuration stored in EEPROM.

WRITE-PROTECT PIN

The WP pin allows the user to write-protect the LTC2978's configuration registers. The WP pin is active high, and when asserted it overrides the WRITE_PROTECT command register. All registers are write-protected by the WP pin except for PAGE, OPERATION, CLEAR_FAULTS, MFR_PAGE_FF_MASK and STORE_USER_ALL.

OTHER OPERATIONS

Clock Sharing

Multiple LTC2978s can synchronize their clocks in an application by connecting together the open-drain SHARE_CLK input/outputs to a pull-up resistor as a wired AND. In this case the fastest clock will take over and synchronize all LTC2978s.

The LTC2978 can be configured to respond to the SHARE_CLK pin being held low by disabling all channels after a brief de-glitch period. When the SHARE_CLK pin is allowed to rise, the LTC2978 will respond by beginning a soft-start sequence.

The LTC2978 can be configured to hold SHARE_CLK low when the unit is off for insufficient input voltage by writing b[3] = 1 "mfr_config_vin_share_enable" of the MFR_CONFIG_ALL register.

APPLICATIONS INFORMATION

LTC2978 Overview

The LTC2978 is a power management IC that is capable of sequencing, margining, trimming, OV/UV supervision, providing fault management, and voltage read back for eight DC/DC converters. Input voltage and temperature read back is also available. Odd numbered channels can be configured to read back sense resistor voltages. Multiple LTC2978s can be synchronized to operate in unison using the SHARE_CLK, FAULTB and CONTROL pins. The LTC2978 utilizes a PMBus compliant interface and command set.

Setting Command Register Values

The command register settings described herein are for the purpose of understanding and software development in a host processor. In actual practice, the LTC2978 can be completely configured for standalone operation with the LTC DC590B dongle and software GUI using intuitive menu driven objects.

Command Units On or Off

Three control parameters determine how a particular channel is turned on and off. The CONTROL*n* pins, the OPERATION command and the value of the input voltage measured at the V_{IN_SNS} pin (V_{IN}). In all cases, V_{IN} must exceed V_{IN_ON} in order to enable a start. When V_{IN} drops below V_{IN_OFF}, an immediate shutdown of all channels will result. Refer to the OPERATION section in the data sheet for a detailed description of the ON_OFF_CONFIG command.

Some examples of typical ON/OFF configurations are:

1. A DC/DC may be configured to turn on anytime V_{IN} exceeds V_{IN_ON}.
2. A DC/DC may be configured to turn on only when it receives an OPERATION command.
3. A DC/DC may be configured to turn on only via the CONTROL pin.
4. A DC/DC may be configured to turn on only when it receives an OPERATION command and the CONTROL pin is asserted.

On Sequencing

The TON_DELAY command sets the amount of time that a channel will wait following the start of an ON sequence before its $V_{OUT\_EN}n$ pin will enable a DC/DC converter. Once the DC/DC converter has been enabled, the TON_RISE command determines the amount of time the LTC2978 waits before the $V_{DACP}n$ output is soft-connected and the DC/DC converter output is servoed to VOUT_COMMAND volts. The TON_MAX_FAULT_LIMIT command determines the amount of time after the DC/DC converter has been enabled that an undervoltage condition will be tolerated before a fault occurs. If a TON_MAX_FAULT occurs, the channel can be configured to disable the DC/DC converter and propagate the fault to other channels using the bidirectional FAULTBz*n* pins. Figure 11 shows a typical on-sequence using the CONTROL pin.

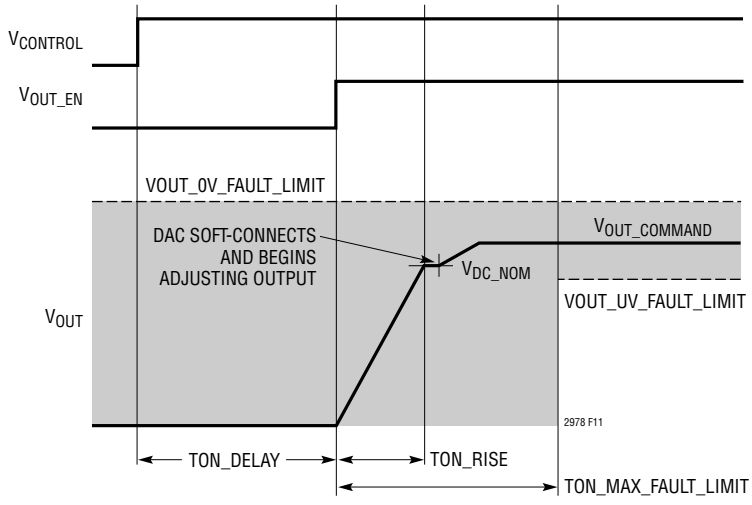


Figure 11. Typical On Sequence Using Control Pin

APPLICATIONS INFORMATION

ON State Operation

Once a channel has reached the ON state, the OPERATION command can be used to command the DC/DC converter's output to margin high, margin low, or return to a nominal output voltage indicated by VOUT_COMMAND. The user also has the option of configuring a channel to continuously trim the output of the DC/DC converter to the VOUT_COMMAND voltage, or the channel's $V_{DACP}n$ output can be placed in a high impedance state thus allowing the DC/DC converter output voltage to go to its nominal value, $V_{DC}n_{(NOM)}$. Refer to the MFR_CONFIG command for details on how to configure the output voltage servo.

Off Sequencing

An off sequence is initiated using the CONTROL*n* pin or the OPERATION command. The TOFF_DELAY command determines the amount of time that elapses from the beginning of the off sequence until each channel's V_{OUT_EN} pin is pulled low thus disabling its DC/DC converter.

V_{OUT} Off Threshold Voltage

The MFR_VOUT_DISCHARGE_THRESHOLD command register allows the user to specify the OFF threshold that the output voltage must decay below before the channel can enter/re-enter the ON state. The OFF threshold voltage is specified by multiplying MFR_VOUT_DISCHARGE_THRESHOLD and VOUT_COMMAND. In the event that an output voltage has not decayed below its OFF threshold before attempting to enter the ON state, the channel will continue to be held off, the appropriate bit is set in the STATUS_MFR_SPECIFIC register, and the ALERTB pin will be asserted low. When the output voltage has decayed below its OFF threshold, the channel can enter the ON state.

Automatic Restart via MFR_RESTART_DELAY Command

If the CONTROL*n* pin is toggled quickly (>10µs deglitch), an automatic restart sequence can be triggered using the MFR_RESTART_DELAY command for the channels enabled by the CONTROL*n* pin (see Figure 12).

V_{OUT} OV/UV Faults

The high speed voltage supervisor OV and UV fault thresholds are configured using the VOUT_OV_FAULT_LIMIT and VOUT_UV_FAULT_LIMIT commands, respectively. The VOUT_UV_FAULT_RESPONSE and VOUT_UV_FAULT_RESPONSE commands determine the response to an OV/UV fault. Fault responses can range from disabling the DC/DC converter immediately, waiting to see if the fault condition persists for some interval before disabling the DC/DC converter, or allowing the DC/DC converter to continue operating in spite of the fault. If a DC/DC converter is disabled, the LTC2978 can be configured to retry or latch-off. The retry interval is specified using the MFR_RETRY_DELAY command. Latched faults are reset by toggling the CONTROL*n* pin, using the OPERATION command, or removing and reapplying the bias voltage (V_{IN_SNS} pin). All fault and warning conditions result in the ALERTB pin being asserted low and the corresponding bits being set in the status registers. The CLEAR_FAULTS command resets the contents of the status registers and deasserts the ALERTB output.

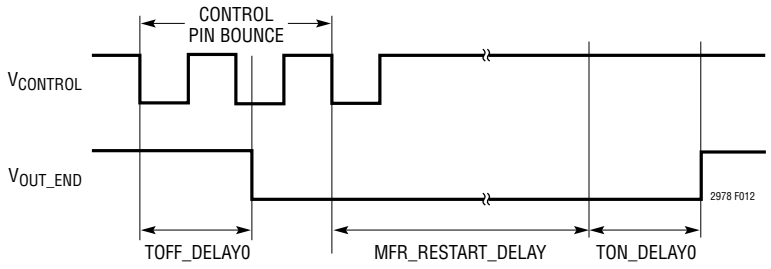


Figure 12. Off Sequence with Automatic Restart

APPLICATIONS INFORMATION

V_{OUT} OV/UV Warnings

OV and UV warning threshold voltages are processed by the LTC2978's ADC. These thresholds are set by the VOUT_OV_WARN_LIMIT and VOUT_UV_WARN_LIMIT commands. If a warning occurs, the corresponding bits are set in the status registers and the ALERTB output is asserted low. Note that a warning will never cause a VOUT_EN*n* output to disable a DC/DC converter.

Configuring the V_{IN_EN} Output

The V_{IN_EN} output may be used to disable the intermediate bus voltage in the event of an output OV or UV fault. Use the MFR_VINEN_OV_FAULT_RESPONSE and MFR_VINEN_UV_FAULT_RESPONSE registers to configure the V_{IN_EN} pin to assert low in response to VOUT_OV/UV fault conditions. The V_{IN_EN} output will stop pulling low when the LTC2978 is commanded to re-enter the ON state following a faulted-off condition.

A charge-pumped 5µA pull-up to 12V is also available on the V_{IN_EN} output. Refer to the MFR_CONFIG_ALL register description in the OPERATION section for more information.

Figure 23 shows an application circuit where the V_{IN_EN} output is used to trigger a SCR crowbar on the intermediate bus in order to protect the DC/DC converter's load from a catastrophic fault such as a stuck top gate.

Multichannel Fault Management

Multichannel fault management is handled using the bidirectional FAULTBz*n* pins. The "z" designates the fault zone which is either 0 or 1. There are two fault zones in the LTC2978. Each zone contains 4-channels. Figure 13 illustrates the connections between channels and the FAULTBz*n* pins.

- The MFR_FAULTBz0_PROPAGATE command acts like a programmable switch that allows faulted-off conditions from a particular channel (PAGE) to propagate to either FAULTBz*n* output in that channel's zone. The MFR_FAULTBz*n*_RESPONSE command controls similar switches on the inputs to each channel that allow any channel to shut down in response to any combination of the FAULTBz*n* pins within a zone. Channels responding to a FAULTBz*n* pin pulling low will attempt a new start sequence when the FAULTBz*n* pin in question is released by the faulted channel.
- To establish dependencies across fault zones, tie the fault pins together, e.g., FAULTB01 to FAULTB10. Any channel can depend on any other. To disable all channels in response to any channel faulting off, short all the FAULTBz*n* pins together, and set MFR_FAULTBz*n*_PROPAGATE = 'h01 and MFR_FAULTBz*n*_RESPONSE = 'h0F for all channels.
- A FAULTBz*n* pin can also be asserted low by an external driver in order to initiate an immediate off-sequence after a 10µs deglitch delay.

APPLICATIONS INFORMATION

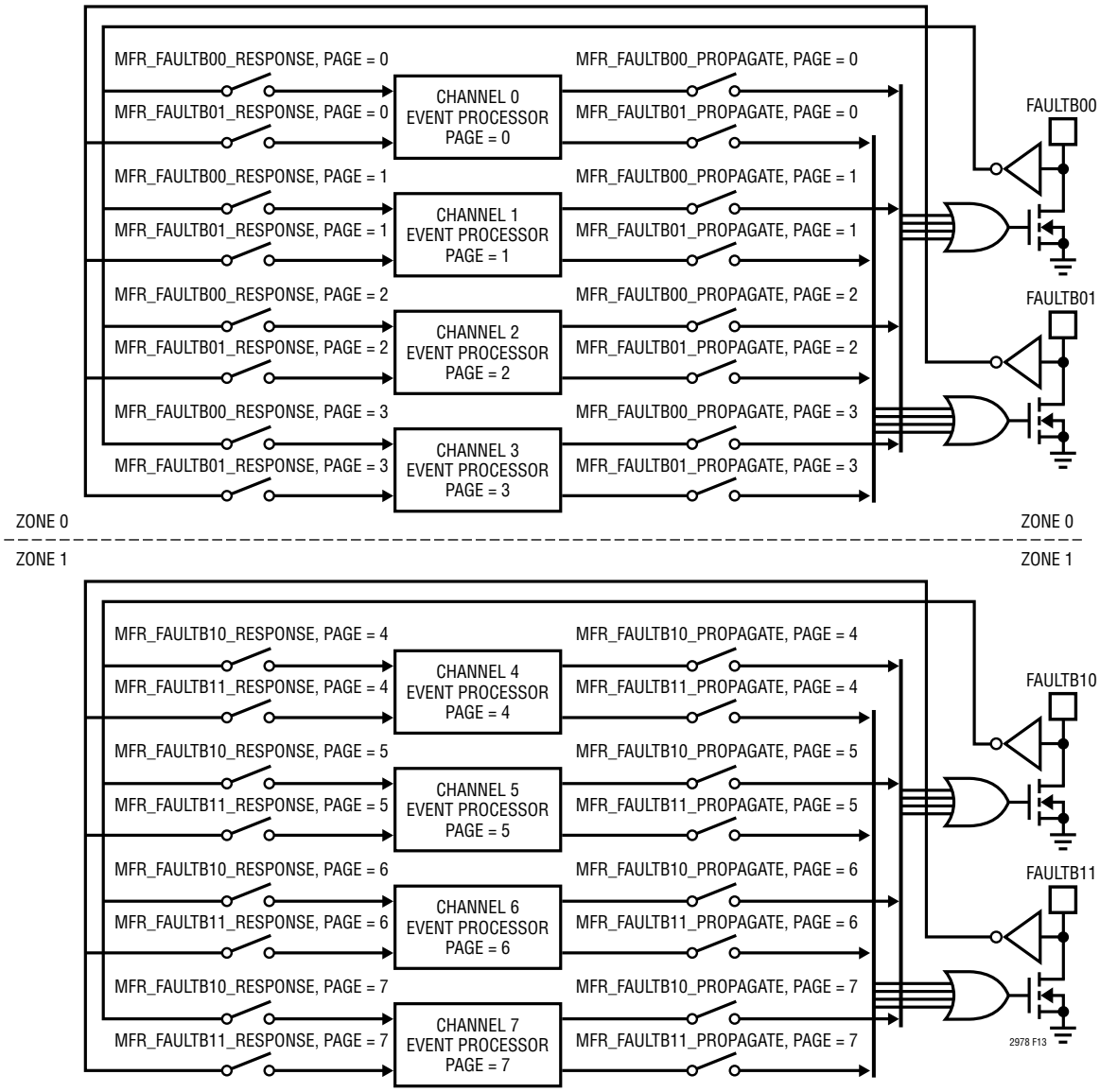


Figure 13. Channel Fault Management Block Diagram

APPLICATIONS INFORMATION

Interconnect Between Multiple LTC2978s

Figure 14 shows how to interconnect the pins in a typical multi-LTC2978 array.

- All V_{IN_SNS} lines should be tied together in a star type connection at the point where V_{IN} is to be sensed. This will minimize timing errors for the case where the ON_OFF_CONFIG is configured to start the LTC2978 based on V_{IN} and ignore the CONTROL*n* line and the OPERATION command. In multi-part applications that are sensitive to timing errors, it is recommended that the Vin_share_enable bit of the MFR_CONFIG_ALL register be set high in order to allow SHARE_CLK to synchronize on/off sequencing in response to the V_{IN_ON} and V_{IN_OFF} thresholds.
- Connecting all V_{IN_EN} lines together will allow an overvoltage (OV) fault on any DC/DC converter's output in the array to shut off a common input switch.
- ALERTB is typically one line in an array of PMBus converters. The LTC2978 allows a rich combination of faults and warnings to be propagated to the ALERTB pin.
- WDI/$\overline{\text{RESET}}$ can be used to put the LTC2978 in the power-on reset state. Pull WDI/$\overline{\text{RESET}}$ low for at least t_{RESETB} to enter this state.
- The FAULTBz*n* lines can be connected together to create fault dependencies. Figure 14 shows a configuration where a fault on any FAULTBz*n* will pull all others low. This is useful for arrays where it is desired to abort a startup sequence in the event any channel does not come up (see Figure 15).
- PWRGD reflects the status of the outputs that are mapped to it by the MFR_PWRGD_EN command. Figure 14 shows all the PWRGD pins connected together, but any combination may be used.

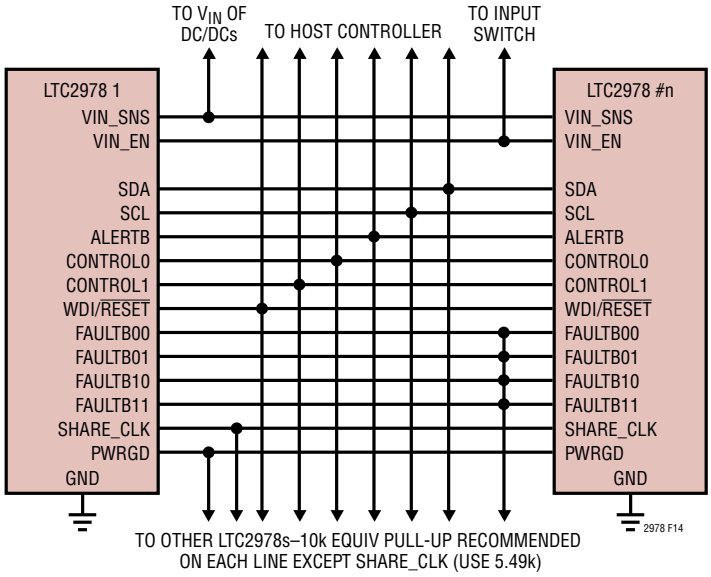


Figure 14. Typical Connections Between Multiple LTC2978s

APPLICATIONS INFORMATION

Trimming and Margining DC/DC Converters with External Feedback Resistors

Figure 16 shows a typical application circuit for trimming/margining a power supply with an external feedback network. The $V_{SENSEP0}$ and $V_{SENSEM0}$ differential inputs sense the load voltage directly, and a correction voltage is developed between the V_{DACP0} and V_{DACM0} pins by the closed-loop servo algorithm. V_{DACM0} is Kelvin connected to the point-of-load GND in order to minimize the effects of load induced grounding errors. The V_{DACP0} output is connected to the DC/DC converter's feedback node through resistor R30.

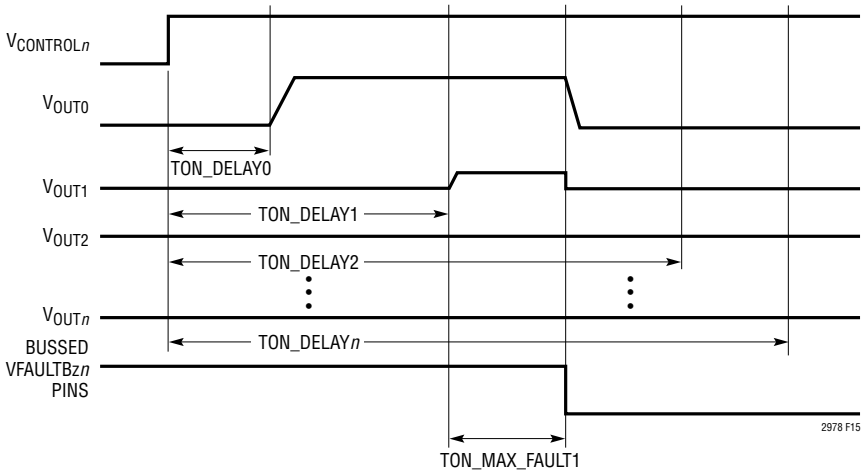


Figure 15. Aborted On Sequence Due to Channel 1 Short

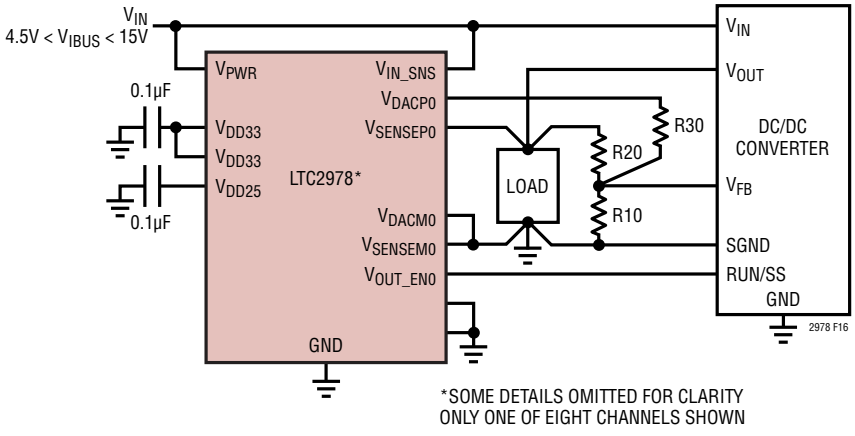


Figure 16. Application Circuit for DC/DC Converters with External Feedback Resistors

APPLICATIONS INFORMATION

4-Step Resistor Selection Procedure for DC/DC Converters with External Feedback Resistors

The following 4-step procedure should be used to calculate the resistor values required for the application circuit shown in Figure 16.

1. Assume values for feedback resistor R20 and the nominal DC/DC converter output voltage $V_{DC0(NOM)}$, and solve for R10.

   $V_{DC0(NOM)}$ is the output voltage of the DC/DC converter when the LTC2978's V_{DACP0} pin is in a high impedance state. R10 is a function of R20, $V_{DC0(NOM)}$, the voltage at the feedback node (V_{FB}) when the loop is in regulation, and the feedback node's input current (I_{FB}).

$$R10 = \frac{R20 \bullet V_{FB0}}{V_{DC(NOM)} - I_{FB0} \bullet R20 - V_{FB}} \quad (1)$$

2. Solve for the value of R30 that yields the maximum required DC/DC converter output voltage $V_{DC0(MAX)}$.

   When V_{DACP0} is at 0V, the output of the DC/DC converter is at its maximum voltage.

$$R30 \leq \frac{R20 \bullet V_{FB}}{V_{DC(MAX)} - V_{DC(NOM)}} \quad (2)$$

3. Solve for the minimum value of V_{DACP0} that's needed to yield the minimum required DC/DC converter output voltage $V_{DC0(MIN)}$.

   The voltage-buffered current DAC has two full-scale settings, 1.33V ±3.7% and 2.7V ±3.7%. In order to select the appropriate full-scale setting, calculate the maximum required V_{DACOP} output voltage:

$$V_{DACP0} > \left(V_{DC(NOM)} - V_{DC(MIN)}\right) \bullet \frac{R30}{R20} + V_{FB} \quad (3)$$

4. Recalculate the minimum, nominal, and maximum DC/DC converter output voltages and the resulting margining resolution.

$$V_{DC(NOM)} = V_{FB} \bullet \left(1 + \frac{R20}{R10}\right) + I_{FB} \bullet R20 \quad (4)$$

$$V_{DC0(MIN)} = V_{DC0(NOM)} - \frac{R20}{R30} \bullet \left(V_{DACP0(F/S)} - V_{FB}\right) \quad (5)$$

$$V_{DC0(MAX)} = V_{DC(NOM)} + \frac{R20}{R30} \bullet V_{FB} \quad (6)$$

$$V_{RES} = \frac{\frac{R20}{R30} \bullet V_{DACP0(F/S)}}{1024} \text{ V/DAC LSB} \quad (7)$$

APPLICATIONS INFORMATION

Trimming and Margining DC/DC Converters with a TRIM Pin

Figure 17 illustrates a typical application circuit for trimming/margining the output voltage of a DC/DC converter with a TRIM Pin. The LTC2978's V_{DACPn} pin connects to the TRIM pin through resistor R30, and the V_{DACM0} pin is connected to the converter's point-of-load ground.

DC/DC converters with a TRIM pin are typically margined high or low by connecting an external resistor between the TRIM pin and either the V_{SENSEP} or V_{SENSEM} pin. The relationships between these resistors and the Δ% change in the output voltage of the DC/DC converter are typically expressed as:

$$R_{TRIM\_DOWN} = \frac{R_{TRIM} \bullet 50}{\Delta_{DOWN}\%} - R_{TRIM} \quad (8)$$

$$R_{TRIM\_UP} =$$

$$R_{TRIM} \bullet \left[\frac{V_{DC} \bullet (100 + \Delta_{UP}\%)}{2 \bullet V_{REF} \bullet \Delta_{UP}\%} - \left(\frac{50}{\Delta_{UP}\%} \right) - 1 \right] \quad (9)$$

where R_{TRIM} is the resistance looking into the TRIM pin, V_{REF} is the TRIM pin's open-circuit output voltage and V_{DC} is the DC/DC converter's nominal output voltage. Δ_{UP}% and Δ_{DOWN}% denote the percentage change in the converter's output voltage when margining up or down, respectively.

2-Step Resistor and DAC Full-Scale Voltage Selection Procedure for DC/DC Converters with a TRIM Pin

The following 2-step procedure should be used to calculate the resistor value for R30 and the required full-scale DAC voltage (refer to Figure 17).

1. Solve for R30:

$$R30 \le R_{TRIM} \bullet \left(\frac{50 - \Delta_{DOWN}\%}{\Delta_{DOWN}\%} \right) \quad (10)$$

2. Calculate the maximum required output voltage for V_{DACP0}:

$$V_{DACP0} \ge \left(1 + \frac{\Delta_{UP}\%}{\Delta_{DOWN}\%} \right) \bullet V_{REF} \quad (11)$$

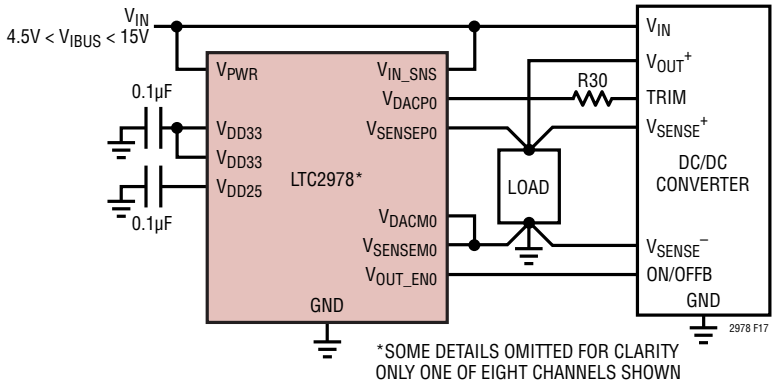


Figure 17. Application Circuit for DC/DC Converters with Trim Pin

APPLICATIONS INFORMATION

Measuring Current

Odd numbered ADC channels may be used to measure supply current. Set the ADC to high resolution mode to configure for current measuring and improve sensitivity. Note that no OV or UV faults or warnings are reported in this mode, but telemetry is available from the READ_VOUT command using the 11-bit signed mantissa plus 5-bit signed exponent linear data format. Set the MFR_CONFIG bit b[9] = 1 in order to enable high res mode. Note: Any channel configured for ADC high res mode should be permanently commanded off, i.e., OPERATION register = 'h00 (this is the factory default EEPROM value). The $V_{OUT\_EN}n$ will assert low in this mode and cannot be used to control a DC/DC. The $V_{DACP}n$ output is also unavailable.

A circuit for measuring current is shown in Figure 18. The balanced filter, R_{CM}, C_{CM}, rejects common mode and differential mode noise from the inductor of the switching DC/DC converter. The filter to the ADC is placed directly across the inductor or a sense resistor in series with the inductor. Note that the + input to the ADC must be limited to <6V above ground. Select R_{CM} and C_{CM} such that the corner frequency is ≤1/10 the DC/DC converter switching frequency and ≤1/10 of the internal 62.5kHz clock of the LTC2978's ΔΣ ADC. This will assure that the DC value at the (+) input to the ADC will be equal to the output voltage with small ripple. Good values are R_{CM} = 100Ω, C_{CM} ≥ 1µF. Keep R_{CM} ≤ 100Ω to minimize gain errors due to ADC input resistance.

Many switching regulator control ICs derive AC inductor current information from an RC network such as the one formed by R1, C1, R2 and C2. The proper placement of the balanced common mode filter for the ADC input is also shown in Figure 18.

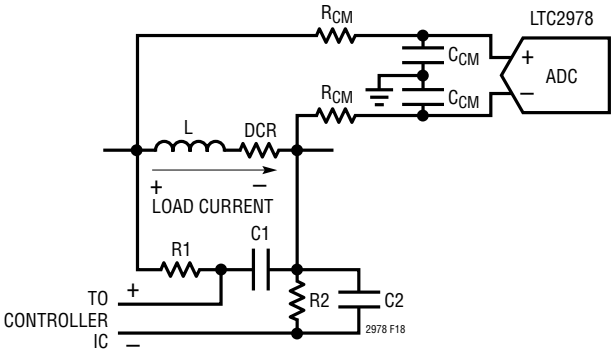


Figure 18. DCR Current Sensing Circuits

APPLICATIONS INFORMATION

Antialiasing Filter Considerations

Extremely noisy environments may require an antialiasing filter on the input to the LTC2978's ADC. The R-C circuit shown in Figure 19 is adequate for most situations. Keep R40 = R50 ≤ 200Ω to minimize ADC gain errors, and select a value for capacitors C10 and C20 that doesn't add too much additional response time to the OV/UV supervisor, e.g. τ ≅ 10µs (R = 100Ω, C = 0.10µF).

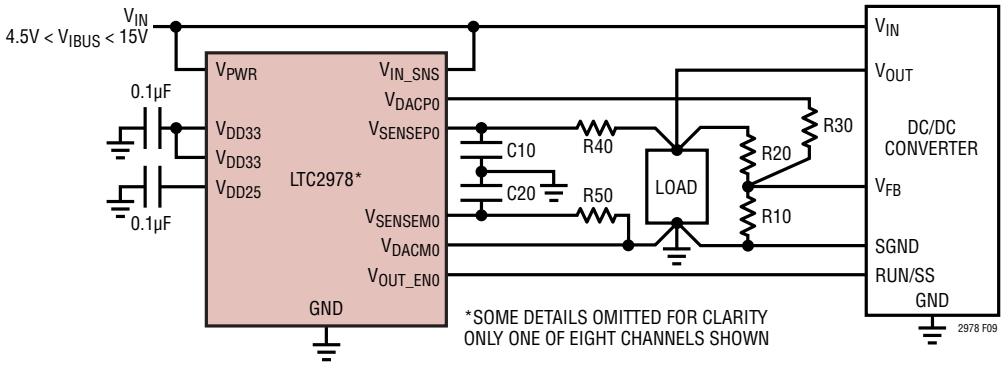


Figure 19. Antialiasing Filter on V_{SENSE} Lines

APPLICATIONS INFORMATION

Dongle Connections

Figure 20 illustrates the application schematic for powering and programming one or more LTC2978's from the LTC PMBus controller in the absence of system power. Because of the controller's limited current sourcing capability, only the LTC2978's and the I^2C pull-up resistors should be powered from the ORed 3.3V supply. In addition, any device sharing I^2C bus connections with the LTC2978 should not have body diodes between the SDA/SCL pins and its V_{DD} node because this will interfere with bus communication in the absence of system power.

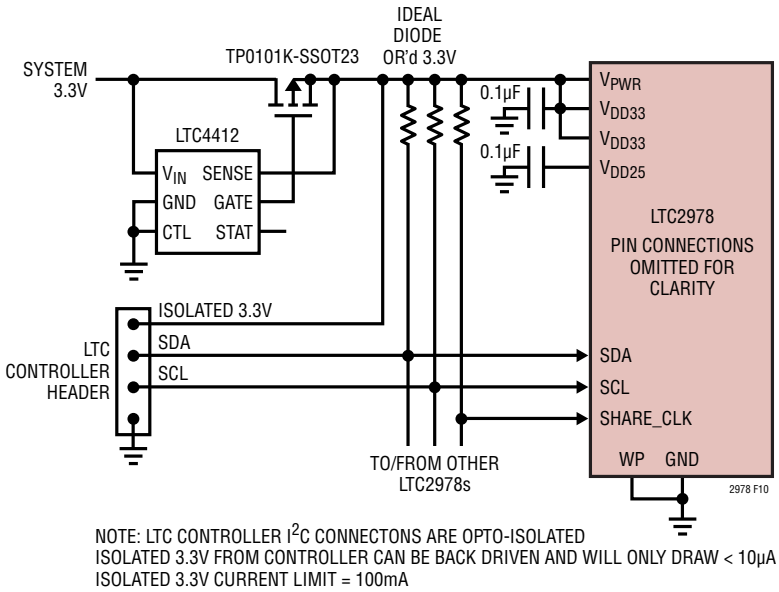


Figure 20. LTC Controller Connections for Powering and Communicating with the LTC2978

APPLICATIONS INFORMATION

PCB ASSEMBLY AND LAYOUT SUGGESTIONS

Bypass Capacitor Placement

The LTC2978 requires 0.1µF bypass capacitors between the V_{DD33} pins and GND, the V_{DD25} pin and GND, and the REFP pin and REFM pin. If the chip is being powered from the V_{PWR} input, then that pin should also be bypassed to GND by a 0.1µF capacitor. In order to be effective, these capacitors should be made of high quality ceramic dielectric such as X5R or X7R and be placed as close to the chip as possible.

Exposed Pad Stencil Design

The LTC2978's package is thermally and electrically efficient. This is enabled by the exposed die attach pad on the under side of the package which must be soldered down to the PCB or mother board substrate. It is a good practice to minimize the presence of voids within the exposed pad inter-connection. Total elimination of voids is difficult, but the design of the exposed pad stencil is key. Figure 21 shows a suggested screen print pattern. The proposed stencil design enables out-gassing of the solder paste during reflow as well as regulating the finished solder thickness.

PC Board Layout

Mechanical stress on a PC board and soldering-induced stress can cause the LTC2978's reference voltage and voltage drift to shift. A simple way to reduce these stress-related shifts is to mount the IC near the short edge of the PC board, or in a corner. The board edge acts as a stress boundary, or a region where the flexure of the board is minimal.

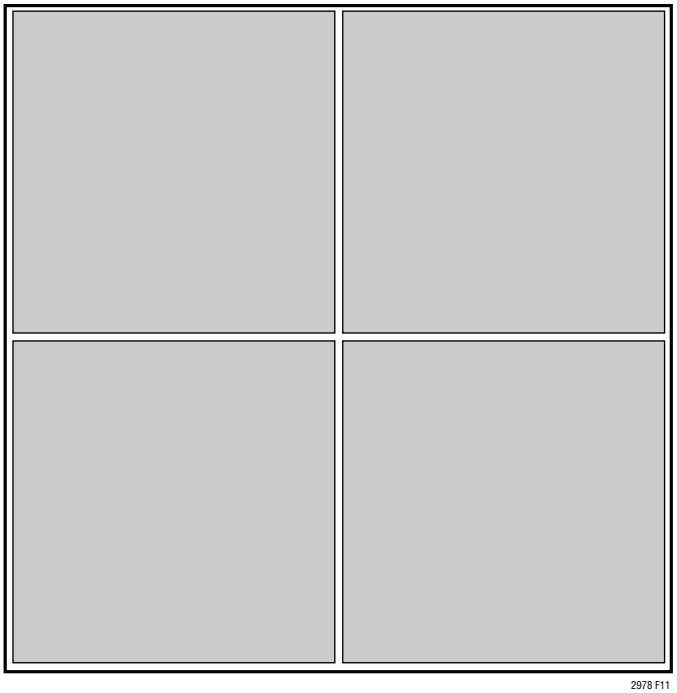


Figure 21. Suggested Screen Pattern for Die Attach Pad

TYPICAL APPLICATION

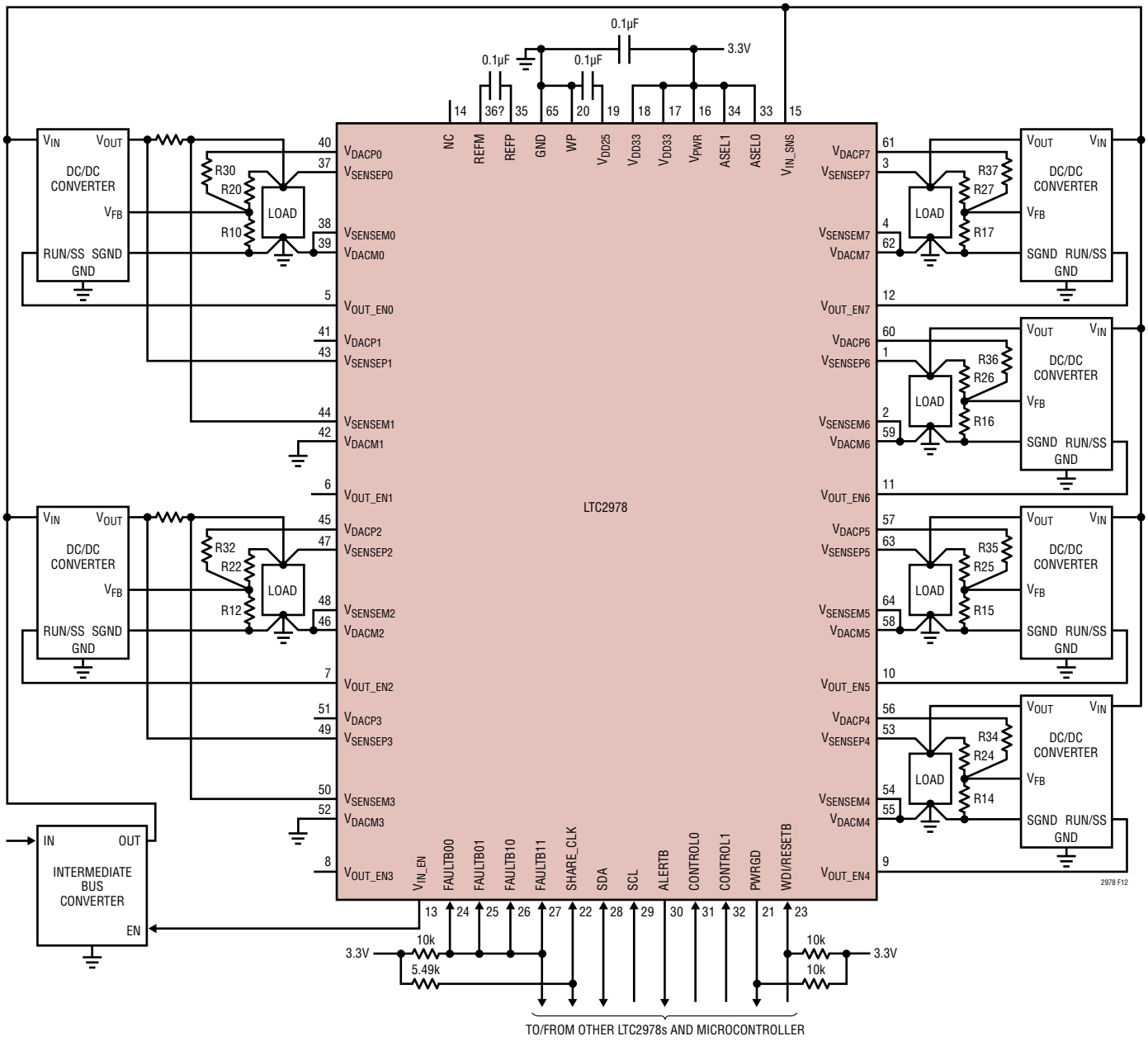
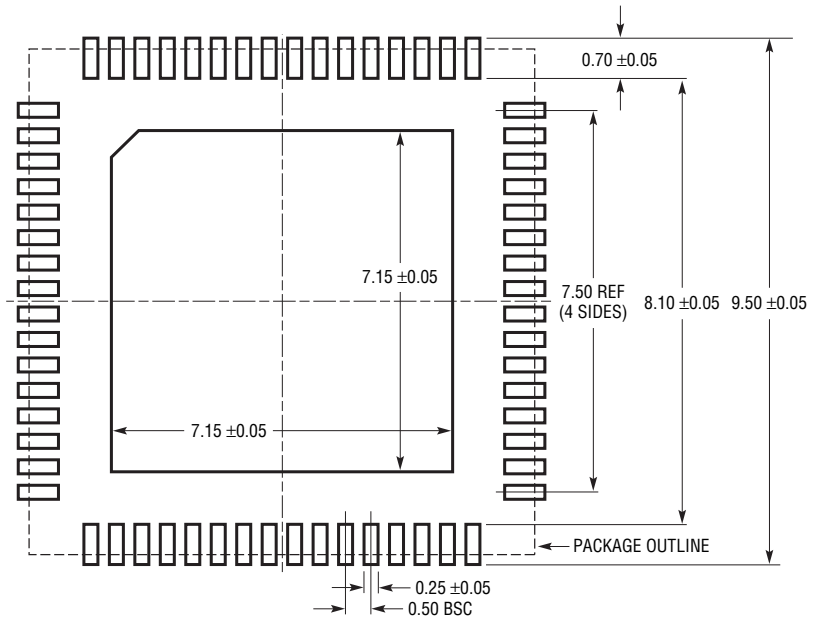


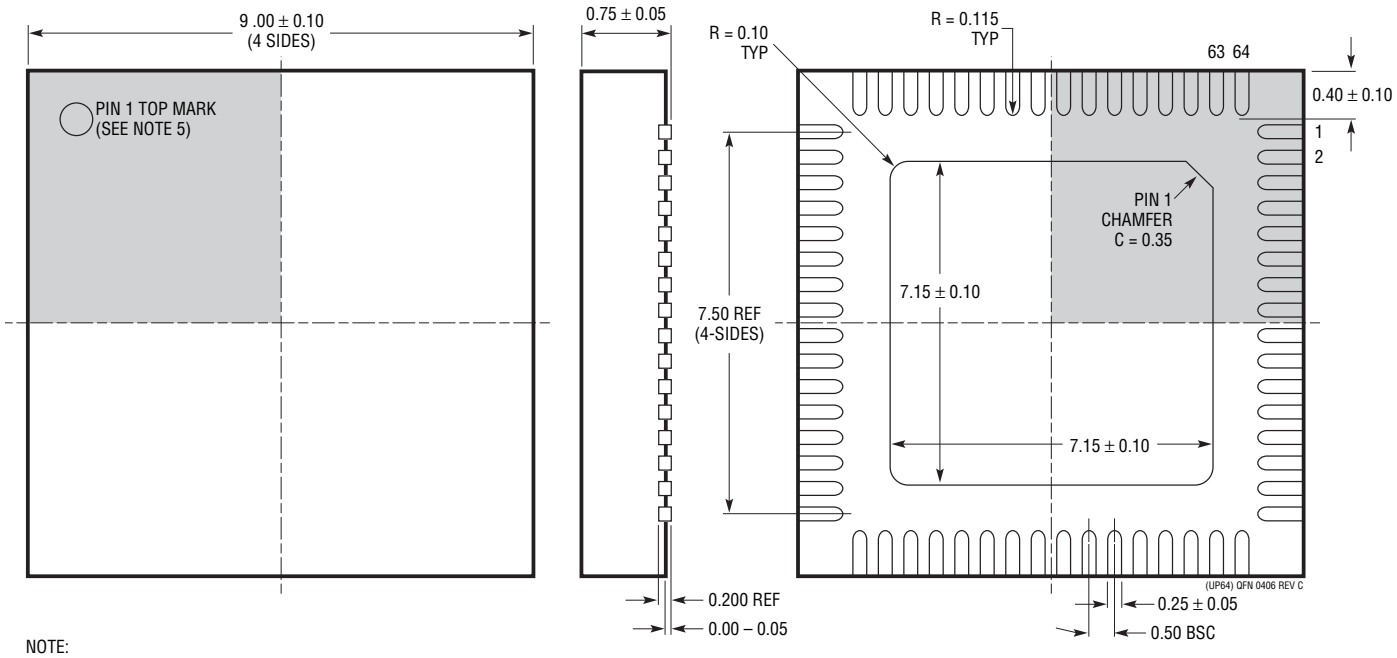
Figure 22. LTC2978 Application Circuit with 3.3V Chip Power

PACKAGE DESCRIPTION

UP Package
64-Lead Plastic QFN (9mm × 9mm)
(Reference LTC DWG # 05-08-1705 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION WNJR-5
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE, IF PRESENT
4. EXPOSED PAD SHALL BE SOLDER PLATED
5. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE
6. DRAWING NOT TO SCALE

TYPICAL APPLICATION

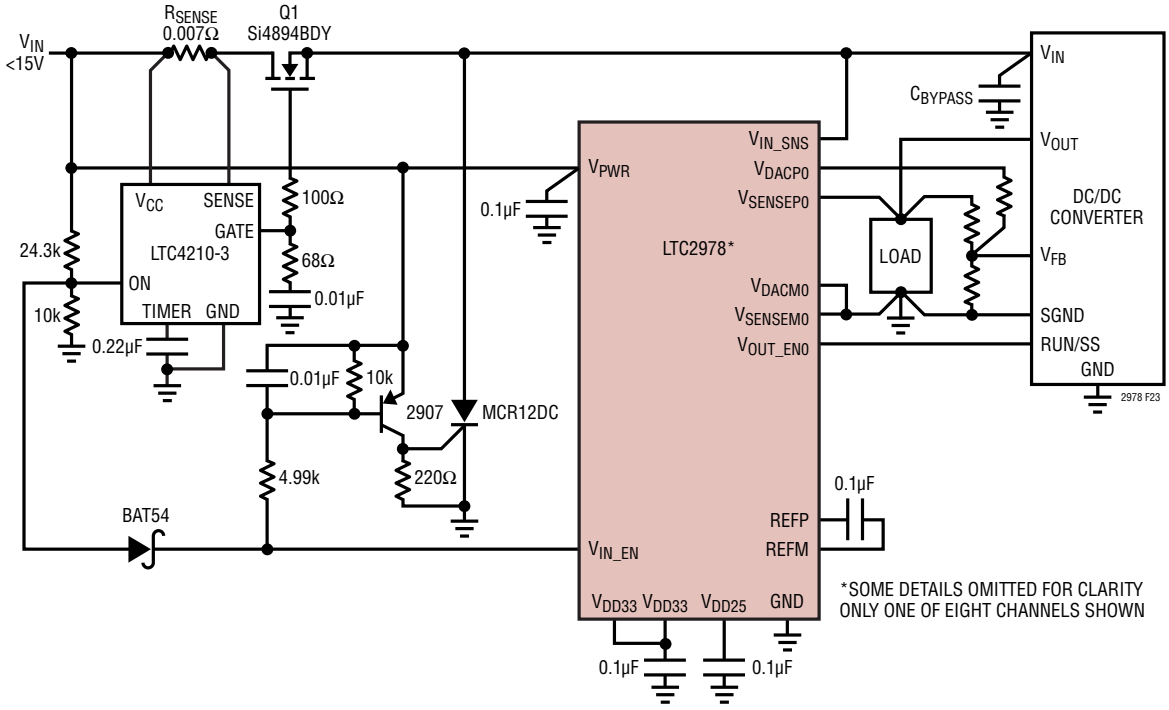


Figure 23. LTC2978 Application Circuit with Crowbar Protection on Intermediate Bus

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC2970	Dual I^2C Power Supply Monitor and Margining Controller	14-Bit ΔΣ ADC with < ±0.5% TUE, Dual 8-Bit IDACs with 1x Voltage Buffers
LTC4151	High Voltage I^2C Current and Voltage Monitor	7V to 80V, 12-Bit Resolution
LTC4210-3	Hot Swap™ Controller in 6-Lead SOT-23 Package	Adjustable Analog Current Limit with Circuit Breaker, Fast Response Limits Peak Fault Current
LTC4412	Low Loss PowerPath™ Controller in ThinSOT™	Replaces Power Supply ORing Diodes, Minimal External Components, Automatic Switching Between DC Sources, Simplifies Load Sharing with Multiple Batteries, Low Quiescent Current: 11µA
LTM®4601	8A, Low V_{IN} DC/DC µModule® with PLL, Output Tracking and Margining	Complete Switch Mode Power Supply, 4.5V to 20V Input Voltage, 0.6V to 5V Output Voltage, PLL Frequency Synchronization, ±1.5% Regulation
LTM4608	8A, Low V_{IN} DC/DC µModule with Tracking, Margining, Multiphase and Frequency Synchronization	Complete Switch Mode Power Supply, 2.7V to 5.5V Input Voltage, 0.6V to 5V Output Voltage, Onboard Frequency Synchronization, ±1.5% Regulation

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